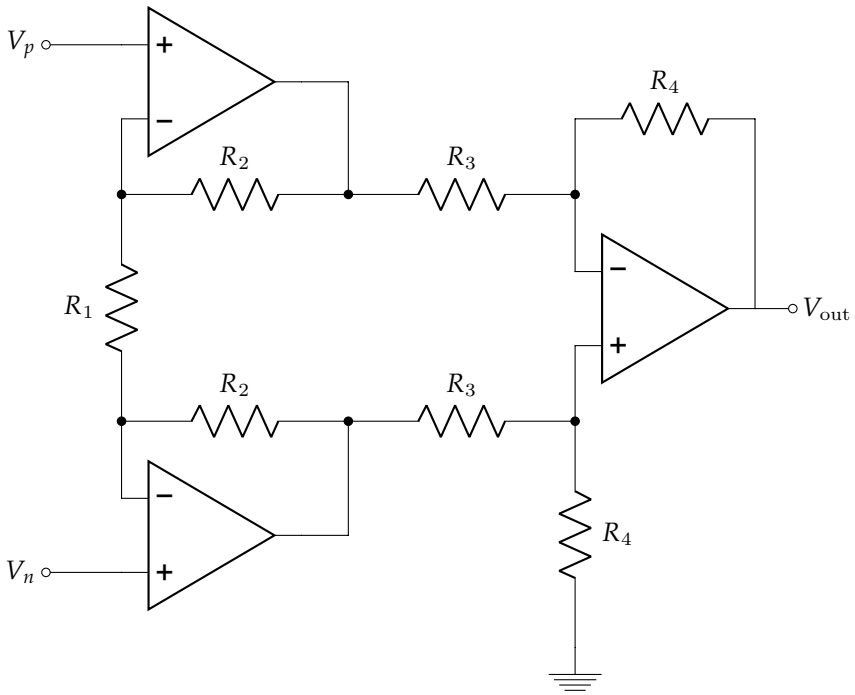
This homework is due on Tuesday, June 30, 2020, at 11:59PM.
Self-grades are due on Tuesday, July 7, 2020, at 11:59PM.

1 Op-Amp Review

Consider the circuit below:

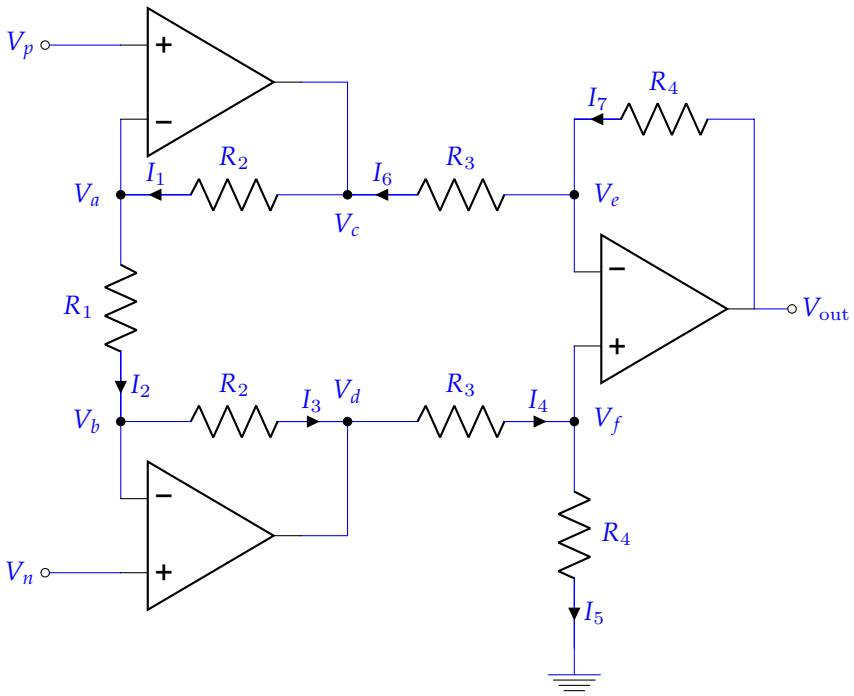


a) Write down all branch and node equations using KCL and the Golden Rules of op-amps.

Solution

For an op-amp in negative feedback, the Golden Rules are (1) the voltage difference between the two inputs is zero ($V^+ = V^-$), and (2) no current goes into the inputs of an op-amp.

Let's label the unknown nodes in this circuit as nodes a through f and branch currents I_1 to I_7. Here, we apply second Golden Rule to have all input currents of op-amps as 0. See the following figure:



According to the first Golden Rule, we can write down:

$$V_a = V_p$$
$$V_b = V_n$$
$$V_e = V_f$$

Then we write down the node current equations based on Kirchhoff's Current Law (KCL) (the sum of total currents flowing into one node is the same as the sum of currents flowing out of that same node.):

$$I_1 = I_2 \implies \frac{V_c - V_p}{R_2} = \frac{V_a - V_b}{R_1} = \frac{V_p - V_n}{R_1}$$
$$I_2 = I_3 \implies \frac{V_a - V_b}{R_1} = \frac{V_p - V_n}{R_1} = \frac{V_n - V_d}{R_2}$$
$$I_4 = I_5 \implies \frac{V_d - V_f}{R_3} = \frac{V_f}{R_4}$$
$$I_6 = I_7 \implies \frac{V_e - V_c}{R_3} = \frac{V_{\text{out}} - V_e}{R_4}$$

You can define currents in whichever directions you like, but you should arrive at the same conclusion that $|I_1| = |I_2| = |I_3|$.

b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two R_2's? How do the currents of R_2's influence the current through R_1?

Solution

According to the branch current equations: $I_1 = I_2$ and $I_2 = I_3$, so the currents going through the two R_2's are the same but with opposite directions: one is from the output

of the op-amp to the inverting input, while the other is from the inverting input to the output. The current through R_1 is the same as the current through the R_2's.

c) What is the current through R_1?

Solution

The current through R_1 is $I_2 = \frac{V_p - V_n}{R_1}$. If $V_p - V_n$ is negative, the current will flow in the opposite direction of what is drawn in the diagram.

d) What are the output voltages of the two op-amps at the first stage?

Solution

For the upper op-amp, $V_c = V_a + I_1 R_2$, where $I_1 = \frac{V_p - V_n}{R_1}$, and $V_a = V_p$. Therefore, the output voltage V_c of the upper op-amp is $V_p + \frac{(V_p - V_n)}{R_1} R_2$.

For the lower op-amp, $V_d = V_b - I_3 R_2$, where $I_3 = \frac{V_p - V_n}{R_1}$, and $V_b = V_n$. Therefore, the output voltage V_d of the lower op-amp is $V_n - \frac{(V_p - V_n)}{R_1} R_2$.

e) Compute the voltage at the + terminal of the second-stage op-amp.

Solution

From part (a), we know that $\frac{(V_d - V_f)}{R_3} = \frac{V_f}{R_4}$. Hence, we could express V_f with V_d as follows:

$$V_f = \frac{R_4}{R_3 + R_4} V_d$$

and plug in the value of V_d we computed in (d), $V_d = V_n - \frac{(V_p - V_n)}{R_1} R_2$:

$$V_f = \frac{R_4}{R_3 + R_4} \left(V_n - \frac{(V_p - V_n)}{R_1} R_2 \right).$$

f) What is V_{out}?

Solution

There are two ways to compute V_{out}: (1) use all known values to derive the answer, or (2) start with V_c and V_d as inputs (free variables) first, and then plug in the values of V_c and V_d in the end of computation. Here we will show you (1), and in part (h), you will see (2).

From part (a) (Golden Rules), we know that $V_e = V_f$, and from part (e), we derived $V_f = \frac{R_4}{R_3 + R_4} \left(V_n - \frac{(V_p - V_n)}{R_1} R_2 \right)$. Also, from part (d), we showed that $V_c = V_p + \frac{(V_p - V_n)}{R_1} R_2$.

From part (a), we know that $\frac{V_e - V_c}{R_3} = \frac{V_{\text{out}} - V_e}{R_4}$. We can express V_{out} in terms of V_e and V_c:

$$V_{\text{out}} = \left(1 + \frac{R_4}{R_3} \right) V_e - \frac{R_4}{R_3} V_c$$

After plugging in the values for V_c and V_e, we get V_{out}:

$$
\begin{aligned}
V_{\text{out}} &= \left(1 + \frac{R_4}{R_3}\right) \frac{R_4}{R_3 + R_4} \left(V_n - \frac{(V_p - V_n)}{R_1} R_2\right) - \frac{R_4}{R_3} \left(V_p + \frac{(V_p - V_n)}{R_1} R_2\right) \\
&= \frac{R_4}{R_3} \left(V_n - V_p - \frac{2R_2(V_p - V_n)}{R_1}\right) \\
&= (V_n - V_p) \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1}\right)
\end{aligned}
$$

g) If we broke R_1 into two series resistors, each with a resistance of $\frac{R_1}{2}$, what is the voltage at the node in between these resistors?

Solution

The voltage across the resistor R_1 is $V_p - V_n$, and the current flowing through R_1 is

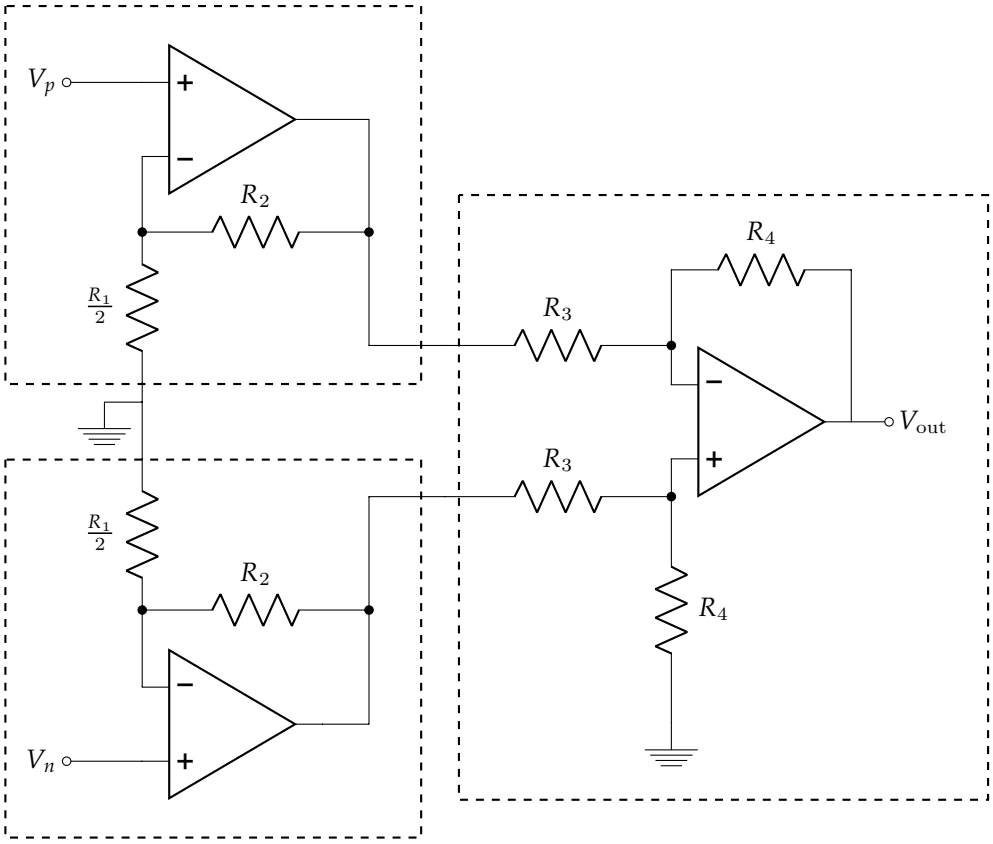
$$\frac{(V_p - V_n)}{R_1}.$$

The voltage in the middle is

$$V_p - \frac{R_1}{2} \frac{(V_p - V_n)}{R_1} = \frac{V_p + V_n}{2}.$$

In other words, it is the average of V_p and V_n.

h) Based on the above analysis, if $V_p = -V_n$, we could introduce a "fake ground" in the middle of the resistor R_1 and come up with the following circuit:



Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks?

What is $\frac{V_{\text{out}}}{V_p - V_n}$ for this revised circuit?

Solution

Usually, we have the DC voltage inputs of V_p and V_n as $V_p = -V_n$. Hence, the voltage in the middle of R_1 is 0. That's why we introduce a fake ground here.

Let's focus on the two op-amps in the first stage: they are exactly the same, except the input voltages. According to the golden rules, the voltage at the $-$ terminal must be the same as at the $+$ terminal. R_2 and $\frac{R_1}{2}$ here are forming voltage dividers for the output voltage of each op-amp. Hence, the gains of the two op-amps are $1 + \frac{2R_2}{R_1}$.

Then, let's take a look at the op-amp in the second stage. Suppose the two inputs for the whole block are V_c and V_d, as we used before. Recall that V_e and V_f must be the same (two inputs of the op-amp).

We have derived $V_e = V_f = \frac{R_4}{R_3+R_4} V_d$ in part (e), and we know that $V_{\text{out}} = \left(1 + \frac{R_4}{R_3}\right) V_e - \frac{R_4}{R_3} V_c$. Replace V_e with $\frac{R_4}{R_3+R_4} V_d$, and we conclude that

$$V_{\text{out}} = \frac{R_4}{R_3}(V_d - V_c).$$

Hence, the gain of the third block in $\frac{R_4}{R_3}$.

Combining the above results, we have $V_{\text{out}} = \frac{R_4}{R_3}(V_d - V_c)$, where $V_c = \left(1 + \frac{2R_2}{R_1}\right) V_p$ and $V_d = \left(1 + \frac{2R_2}{R_1}\right) V_n$. The overall gain is

$$\frac{V_{\text{out}}}{(V_p - V_n)} = -\frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_1}\right).$$

(Check the positions of V_p and V_n.)

This entire circuit is called an instrumentation amplifier, which is the descendant of a combo of two unity gain amplifiers followed by a differential amplifier.

2 Existence and uniqueness of solutions to differential equations

Let's show that if any function x satisfies

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \alpha x(t) \tag{1}$$

as well as

$$x(0) = x_0, \tag{2}$$

then it is unique: if y is *any function* that meets these two criteria then $x = y$.

In order to do this, we will first verify that a solution exists. Then we will compare it to a hypothetical alternative solution—and our goal will to be establish that these two solutions are equal.

a) **Verify that $x_d(t) = x_0 e^{\alpha t}$ satisfies (1) and (2).** (For this proof, x_d will be the "reference solution" against which alternates will be compared.)

Solution

Taking the derivative of $x_d(t)$ with respect to t gives $\alpha x_0 e^{\alpha t}$ by the chain rule, and this is equal to $\alpha x_d(t)$ by inspection. So (1) is satisfied.

Evaluating $x_d(0) = x_0 e^{\alpha \cdot 0} = x_0$ and so (2) is also satisfied.

b) To show that this solution is in fact unique, we need to consider a hypothetical $y(t)$ that also satisfies (1) and (2).

Our goal is to show that $y(t) = x(t)$ for all $t \geq 0$. (The domain $t \geq 0$ is where we have defined the conditions (1) and (2). Outside of that domain, we don't have any constraints.)

How can we show that two things are equal? In the past, you have probably shown that two quantities or functions are equal by starting with one of them, and then manipulating the expression for it using valid substitutions and simplifications until you get the expression for the other one. However, here, we don't have an expression for $y(t)$ so that style of approach won't work.

In such cases, we basically have a couple of basic ways of showing that two things are the same.

- Take the difference of them, and somehow argue that it is 0.
- Take the ratio of them, and somehow argue that it is 1.

We will follow the ratio approach in this problem. First assume that $x_0 \neq 0$. In this case, we are free to define $z(t) = \frac{y(t)}{x_d(t)}$ since we are dividing by something other than zero.

What is $z(0)$?

Solution

We know $z(0) = \frac{y(0)}{x_d(0)} = \frac{x_0}{x_0} = 1$ since $y(0) = x_0$ by (2) and plugging in 0 for t into the exact expression for $x_d(t)$.

c) **Take the derivative $\frac{d}{dt}z(t)$ and simplify using (1) and what you know about the derivative of $x_d(t)$.**

(HINT: The quotient rule for differentiation might be helpful since a ratio is involved.)

Solution

The quotient rule tells us how to take the derivative of $\frac{y}{x_d}$ (we can also view this using the product rule, which is also just another manifestation of the chain rule for differentiation in the multivariate case). The rule applies because the functions involved are differentiable by definition and the denominator is nonzero.

$$\frac{d}{dt}z(t) = \frac{d}{dt}\frac{y(t)}{x_d(t)} = \frac{\frac{d}{dt}y(t)x_d(t) - y(t)\frac{d}{dt}x_d(t)}{(x_d(t))^2} \tag{3}$$

$$= \frac{\alpha y(t)x_d(t) - y(t)\alpha x_d(t)}{(x_d(t))^2} \tag{4}$$

$$= \frac{0}{(x_d(t))^2} = 0 \tag{5}$$

Notice that here, what is important is that both y and x_d satisfy (1) and so the numerator in the quotient rule cancels out to zero. The details of $x_d(t)$ didn't end up mattering.

You should see that this derivative is always 0 and hence $z(t)$ does not change. **What does that imply for y and x_d ?**

Solution

Since $z(t)$ has zero derivative, it cannot change, and hence it stays at its initial value, which is 1. So it is always 1 and hence $\frac{y(t)}{x_d(t)} = 1$ so $y(t) = x_d(t)$.

d) At this point, we have shown uniqueness in most cases. Just one special case is left: $x_0 = 0$. The ratio technique omitted this case, because as $x_d(t) = 0$, x_d cannot be the denominator of a fraction.

To complete our proof we must to show that if $x_0 = 0$, then $y(t) = 0$ for all t, and we will do so by assuming that $y(t)$ is not identically 0 for $t > 0$—that is, at some $t_0 > 0$ $y(t_0) = k \neq 0$.

From (2), we know that $y(0) = 0$. In this part, we will try to work backwards in time from the point $t = t_0$ to $t = 0$ and conclude that y violates (2).

Apply the change of variables $t = t_0 - \tau$ to (1) to get a new differential equation for $\widetilde{x}(\tau) = x(t_0 - \tau)$ that specifies how $\frac{d}{d\tau}\widetilde{x}(\tau)$ must relate to $\widetilde{x}(\tau)$. This should hold for $-\infty < \tau \leq t_0$.

Solution

$$\frac{d}{d\tau}\widetilde{x}(\tau) = \frac{d}{d\tau}x(t_0 - \tau) \tag{6}$$

$$= -\alpha x(t_0 - \tau) \tag{7}$$

$$= -\alpha\widetilde{x}(\tau) \tag{8}$$

where the second line used the chain rule for differentiation and (1).

This holds for all $t \geq 0$ which means $t_0 - \tau \geq 0$ which is the same as $\tau \leq t_0$.

e) Because the previous part resulted in a differential equation of a form for which we have already proved uniqueness for the case of nonzero initial condition, and since $\widetilde{y}(0) = y(t_0) = k \neq 0$, we know what $\widetilde{y}(\tau)$ must be. **Write the expressions for $\widetilde{y}(\tau)$ for $\tau \in [0, t_0]$ and what that implies for $y(t)$ for $t \in [0, t_0]$.**

Solution

We know that $\widetilde{y}$ satisfies $\frac{d}{d\tau}\widetilde{y}(\tau) = -\alpha\widetilde{y}(\tau)$ and that $\widetilde{y}(0) = k \neq 0$. Consequently, by the uniqueness theorem already proved, we know that it must be the case that $\widetilde{y}(\tau) = ke^{-\alpha\tau}$ for the range $\tau > 0$ as long as the differential equation is valid.

This means that $y(t) = ke^{-\alpha(t_0-t)}$ as long as $0 \leq t \leq t_0$.

f) **Evaluate $y(0)$ and argue that this is a contradiction for the specified initial condition** (2).

Solution

Evaluating this expression at $t = 0$ gives $y(0) = ke^{-\alpha t_0}$. Because $k \neq 0$, this means $y(0) \neq 0$. This is a contradiction with (2) since that asserts a zero initial condition $x_0 = 0$.

Consequently, such a $y(t)$ cannot exist and only the all zero solution is permitted — establishing uniqueness in this case of $x_0 = 0$ as well.

g) Explain in your own words why it matters that solutions to these differential equations are unique.

Solution

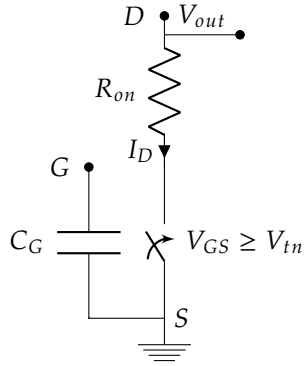
Uniqueness means that we need not continue looking once a satisfactory guess has been reached. If our model had non-unique solutions—such as kinematics problem where the quantity of interest arises as a root of a quadratic—then we would potentially have to choose between multiple, or even infinitely many solutions.

Although we gave you lots of guidance in this problem, we hope that you can internalize this way of thinking.

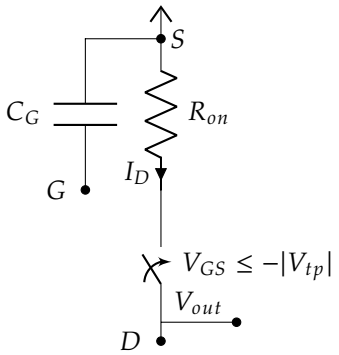
This elementary approach to proving the uniqueness of solutions to differential equations works for the kinds of linear differential equations that we will tend to encounter in EE16B. For more complicated nonlinear differential equations, further conditions are required for uniqueness (appropriate continuity and differentiability) and proofs can be found in upper-division mathematics courses on differential equations when you study the Picard-Lindelöf theorem. (It involves looking at the magnitude of the difference of the two hypothetical solutions and showing this has to be arbitrarily small and hence zero. However, the basic elementary case we have established here can be viewed as a building block — the quotient rule gets invoked in the appropriate place, etc. The additional ingredients that are out-of-scope for lower-division courses are fixed-point theorems — which you can think of as more general siblings of the intermediate-value theorem you saw in basic calculus.)

3 Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitance C_G represents the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model



(b) PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_G = 1\text{fF}$ (femto-Farads = 10^{-15}). We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e. , the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (fig. 2).

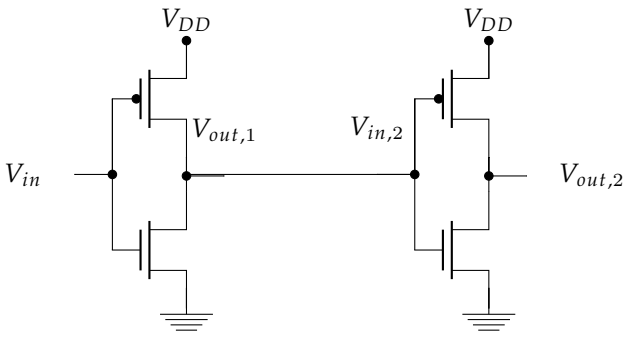


Figure 2: CMOS Inverter chain

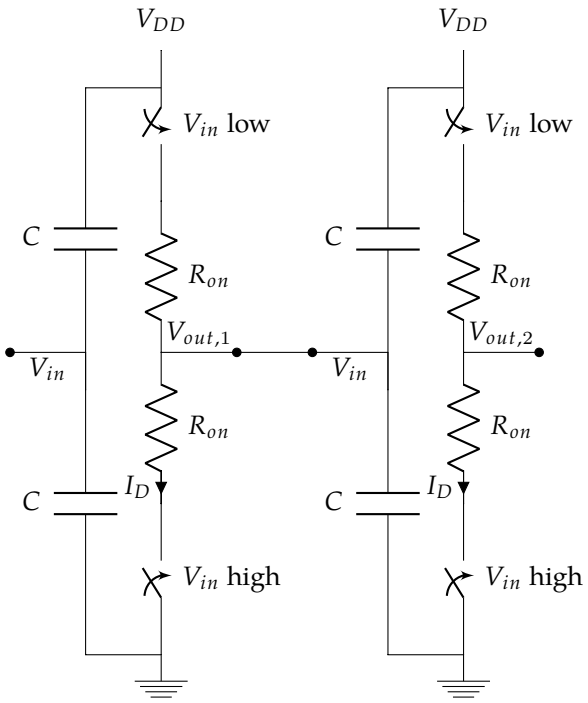


Figure 3: Inverter Transistor Resistor-switch model

a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,1}$) for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

Solution

To analyze this circuit as an RC circuit we can recall the transistor switch model. Using this we can see that the first inverter's output appears as a resistor connected to V_{DD} when the input is low (nmos off, pmos on), or a resistor connected to ground when the input turns high (nmos on, pmos off).

Before $t = 0$, the input to the first inverter was low for a long time. This means that for $t < 0$, the output of the inverter ($V_{out,1}$) had been held at V_{DD} for a long time.

At $t = 0$, the input goes high, which means that the input inverter's nmos device turns on, connecting $V_{out,1}$ to ground through a resistance of R_{on}.

The second inverter "loads" the output of the first inverter. From the notes in the problem, we can model the gates of the transistors as capacitors. These gates together form our capacitive load. The gate of the pmos acts as a capacitor to V_{DD} and the gate of the nmos acts as a capacitor to ground.

Using this we can draw the following RC circuit:

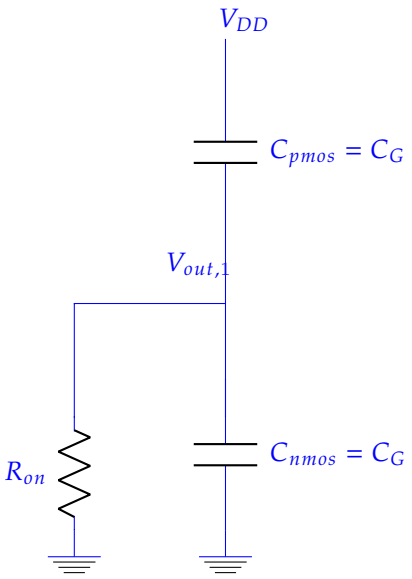


Figure 4: First inverter output at 0

To get the differential equation describing the output of the first inverter at time $t \geq 0$ let us first think about the behavior of the circuit at and after $t = 0$.

Before $t = 0$ we know that the output $V_{out,1} = V_{DD}$. This means that C_{nmos} is charged, while C_{pmos} is not as there is no voltage difference across it.

At $t = 0$, when the input to the first inverter changes (input switches to high), the nmos will turn on, discharging the $V_{out,1}$ node. Thus $V_{out,1}$ will eventually discharge to zero in steady state.

We know the voltage across C_{pmos} is $V_{out,1}(t) - V_{DD}$ and the voltage across C_{nmos} is $V_{out,1}(t)$. Using this information we can set up a differential equation to solve for $V_{out}(t)$:

$$I_{c_{pmos}} = C_{pmos} \frac{d}{dt}(V_{out,1}(t) - V_{DD}) \tag{9}$$

$$I_{c_{nmos}} = C_{nmos} \frac{d}{dt} V_{out,1}(t) \tag{10}$$

$$I_{R_{on}} = \frac{V_{out,1}(t)}{R_{on}} \tag{11}$$

$$I_{c_{pmos}} + I_{c_{nmos}} = -I_{R_{on}} \tag{12}$$

$$C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{nmos}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}} \tag{13}$$

$$C_{pmos}\frac{d}{dt}V_{out,1}(t) + C_{nmos}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}} \tag{14}$$

$$(C_{pmos} + C_{nmos})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}} \tag{15}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}(C_{pmos} + C_{nmos})} \tag{16}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{2R_{on}C_G} \tag{17}$$

b) Given the initial conditions in part (a), **solve for $V_{out,1}(t)$.**

Solution

We know that the solution to a differential equation of the form

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}}{R_{on}(2C_G)}$$

is

$$V_{out,1}(t) = ke^{-\frac{t}{R_{on}(2C_G)}}$$

Plugging in the initial condition $V_{out,1}(0) = V_{DD}$ we find that $V_{out,1}(t) = V_{DD}e^{-\frac{t}{R_{on}(2C_G)}}$.

c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

Solution

(1) We know that the output of our inverter started with the initial value V_{DD}.

(2) Since the differential equation tells us the change in value of $V_{out,1}(t)$ at time t we can simply plug in $t = 0$ into our differential equation to get the initial slope:

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(0)}{R_{on}(C_{nmos} + C_{pmos})} \tag{18}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{DD}}{R_{on}(C_{nmos} + C_{pmos})} \tag{19}$$

Thus the initial slope is $-\frac{V_{DD}}{R_{on}(C_{nmos}+C_{pmos})} = -\frac{V_{DD}}{R_{on}(2C_G)}$

(3) Since the input to the inverter changed from high to low we know the output of the first inverter ($V_{out,1}$) is going to go to 0 in steady state, as this node will be discharged by the first inverter's nmos transistor.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD}e^{-\frac{\infty}{R_{on}(2C_G)}} = 0$.

(4) To approximate when the output will decay to $\frac{1}{3}$ its original value, we use the fact that $e^{-1} = \frac{1}{e} \approx \frac{1}{3}$. We thus want to find when $V_{out,1} = V_{DD}e^{-1}$. This will occur when the e term is raised to -1, which occurs when $t = R_{on}(2C_G) = 2 * 10^{-12}$.

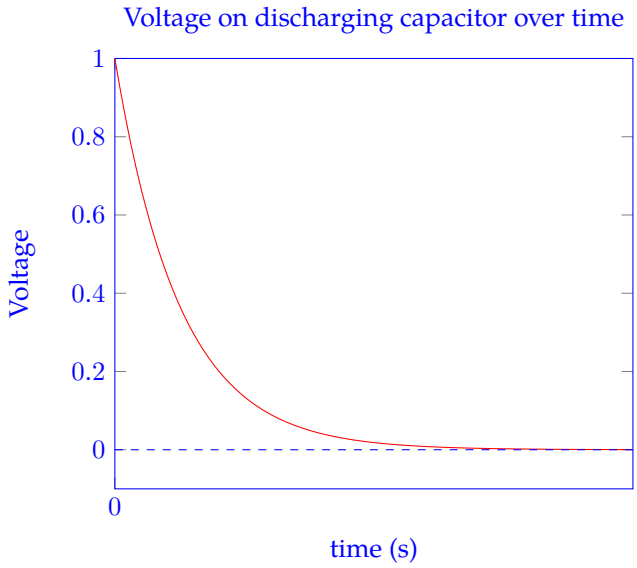


Figure 5

d) A long time later, the input to the first inverter switches low again.
Solve for $V_{out,1}(t)$.
Sketch the output voltage of the first inverter ($V_{out,1}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.

Solution

We know that after a long time, the output of the first inverter has stabilized to 0. When the input switches low again, the input inverter's nmos device turns off, while the input inverter's pmos device turns on. This connects the $V_{out,1}$ node to V_{DD}, as shown in fig. 6.

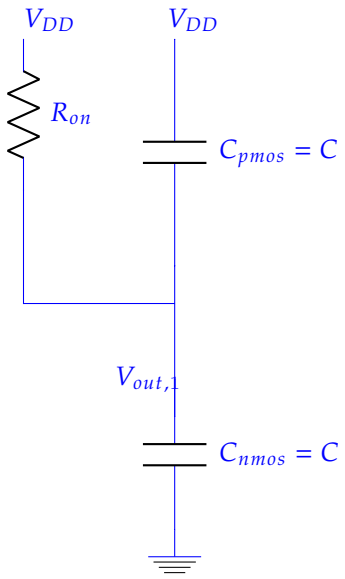


Figure 6: Inverter output at 1

To set up the differential equation, we apply KVL and KCL again:

$$I_{c_{pmos}} = C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \tag{20}$$

$$I_{c_{nmos}} = C_{nmos}\frac{d}{dt}V_{out,1}(t) \tag{21}$$

$$I_{R_{on}} = \frac{V_{out,1}(t) - V_{DD}}{R_{on}} \tag{22}$$

$$I_{c_{pmos}} + I_{c_{nmos}} = -I_{R_{on}} \tag{23}$$

$$C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{nmos}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}} \tag{24}$$

$$C_{pmos}\frac{d}{dt}V_{out,1}(t) + C_{nmos}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}} \tag{25}$$

$$(C_{pmos} + C_{nmos})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}} \tag{26}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}(C_{pmos} + C_{nmos})} \tag{27}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{2R_{on}C_G} \tag{28}$$

We know from lecture that a differential equation of the form $\frac{d}{dt}x(t) + \alpha x(t) = \beta$ has solution

$$x(t) = x_0 e^{-\alpha t} + \frac{\beta}{\alpha}(1 - e^{-\alpha t})$$

Substituting for $x(t) = V_{out,1}, x_0 = 0, \alpha = \frac{1}{2R_{on}C_G}, \beta = \frac{V_{DD}}{2R_{on}C_G}$, we get:

$$V_{out,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{2R_{on}C_G}}\right)$$

(1) Because the input to the first inverter was high for a long time, we know the initial value of $V_{out,1}(t) = 0$. This was the initial condition applied to the solution of the differential equation, above.

(2) To find the initial value of the slope we can plug in $t = 0$ to the above differential equation:

$$\frac{d}{dt}V_{out,1}(t) = \frac{(V_{DD} - V_{out,1}(0))}{R_{on}(2C_G)}$$

where $V_{out,1}(0) = 0$. Thus our initial slope is $\frac{(V_{DD})}{R_{on}(2C_G)}$. Notice this slope is positive while the previous part had a negative slope.

(3) Since the input to the inverter changed from low to high and the input inverter's pmos is now on, we know the output of the first inverter is going to go to V_{DD} in steady state.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD}\left(1 - e^{-\frac{\infty}{R_{on}(2C_G)}}\right) = V_{DD}(1 - 0) = V_{DD}$.

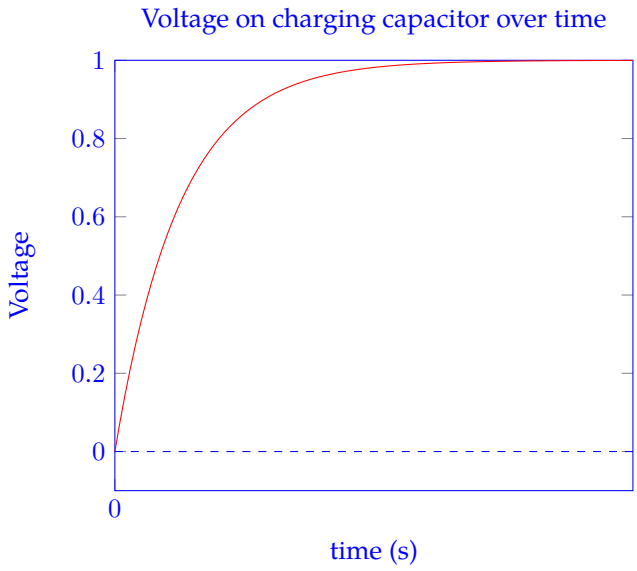


Figure 7

4 CMOS Scaling

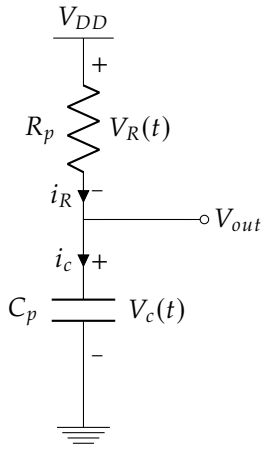
Jerry wants to create a new machine learning accelerator chip using CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transitions and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate). These two parameters are very important for CMOS technology, as they determine how quickly the processor can run and how much power it will consume.

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1\text{V}$. The transistors have a parasitic resistance of $R_p = 10\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5\text{fF}$.

Process B uses a supply voltage of $V_{DD} = 3\text{V}$. The transistors have a parasitic resistance of $R_p = 30\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1\text{fF}$.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:



Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

a) In terms of the variables V_{DD}, R_p, and C_p, **solve for** $V_{out}(t)$.

Solution

To find an expression for $V_{out}(t)$:

$$V_c(t) = V_{out}(t)$$

KCL at V_{out} (note the direction of i_R) yields:

$$i_R(t) = i_c(t)$$

$$\frac{V_{DD} - V_{out}(t)}{R_p} = C_p \frac{dV_{out}(t)}{dt}$$

$$\frac{dV_{out}(t)}{dt} + \frac{1}{R_p C_p} V_{out}(t) = \frac{V_{DD}}{R_p C_p}$$

Using the solution of the differential equation $\frac{d}{dt}x(t) + \alpha x(t) = \beta$ seen in lecture,

$$x(t) = x_0 e^{-\alpha t} + \frac{\beta}{\alpha}(1 - e^{-\alpha t})$$

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)$$

b) Using the expression for $V_{out}(t)$ that was just calculated, **solve for** $i_R(t)$. Keep this expression in terms of the variables V_{DD}, R_p, and C_p.

Solution

$$i_R(t) = \frac{V_{DD} - V_{out}(t)}{R_p} = \frac{V_{DD} - V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)}{R_p} = \frac{V_{DD} e^{-\frac{t}{R_p C_p}}}{R_p}$$

c) In the previous part, you should have noticed that $i_R(t)$ started at some value, and decayed towards 0 as $t \to \infty$.

Why does this trend make sense? If the voltage were switching to a different level, would the same trend in current hold? This question is meant to help build intuition and understanding about switching circuits.

Solution

In steady state (i.e. when $t \to \infty$), we know that the voltage will settle to a constant value. Because $i_C = C\frac{dV_C}{dt}$, it makes sense that when the voltage is constant, the current through the capacitor will be 0. In general, this trend will hold true: when there is a step voltage change (in this case, the transistor suddenly switching on/off) in a circuit with a resistor and capacitor, the current through capacitor will jump to some level ($i_0 = i(t = 0)$), and will then exponentially decay to reach a steady state current of 0.

d) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the time it takes for** V_{out} **to reach** $\frac{V_{DD}}{2}$.

Solution

We can find the delay time by setting $V_{out}(t) = \frac{V_{DD}}{2}$:

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)$$

$$\frac{1}{2} = e^{-\frac{t}{R_p C_p}}$$

$$\ln\left(\frac{1}{2}\right) = -\frac{t}{R_p C_p}$$

$$t = -\ln\left(\frac{1}{2}\right) R_p C_p$$

From this, we can say that the delay time to reach $\frac{V_{DD}}{2}$ for any R_p and C_p is:

$$t_d = 0.69 R_p C_p$$

$$t_d = 0.69(10 \times 10^3 \times 5 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

e) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}.**

For this problem, recall that the instantaneous power delivered by a voltage source is $P(t) = I(t) \cdot V(t)$. Note that the current and voltage are functions of time.

Energy can be found by integrating power:

$$E = \int_{t=0}^{t=\infty} P(t)dt$$

Remember that the units of energy are Joules [J], while the units of power are Watts [W], which is energy per time: $1\text{W} = \frac{1\text{J}}{1\text{s}}$

Solution

The total energy delivered by the source can be found by integrating the instantaneous power:

$$U_s = \int_0^\infty P(t)dt = \int_0^\infty V_{DD} i_R(t)dt$$

$$i_R(t) = C_p \frac{dV_{out}(t)}{dt}$$

$$i_R(t) = C_p V_{DD} \frac{1}{R_p C_p} e^{-\frac{t}{R_p C_p}} = \frac{V_{DD}}{R_p} e^{-\frac{t}{R_p C_p}}$$

$$U_s = \int_0^\infty (V_{DD}) \left(\frac{V_{DD}}{R_p} e^{-\frac{t}{R_p C_p}}\right) dt$$

$$U_R = \int_0^\infty \frac{V_{DD}^2}{R_p} e^{-\frac{t}{R_p C_p}} dt$$

$$U_s = \left(\frac{V_{DD}^2}{R_p}\right)\left(-R_p C\right) e^{-\frac{t}{R_p C_p}} \Bigg|_0^\infty$$

The total energy supplied by the supply when charging up the capacitor is:

$$U_s = C V_{DD}^2$$

Plugging in component values of process A for the energy dissipation and time delay:

$$U_s = (5 \times 10^{-15})1^2 = 5 \times 10^{-15}\text{J}$$

Note: Notice that the energy supplied by the supply when charging the capacitor is $U_s = CV_{DD}^2$. However, we know that the energy stored by a capacitor is $U_{cap} = \frac{1}{2}CV_{DD}^2$. *This implies that the energy drawn from the supply in charging the capacitor is twice the energy that the capacitor finally stores when it is charged.* Where did the other half of the energy go? It is dissipated as heat through the resistor when charging the capacitor. If you do a similar calculation to what you just did, where you integrate the energy dissipated through the resistor as the capacitor is charging (i.e. apply $P = I \cdot V$ to the resistor and integrate), you will find the missing half of the energy.

f) **Repeat parts (d) and (e), but with the values from process B.**

Solution

Using the equations derived above:

$$U_s = (1 \times 10^{-15})3^2 = 9 \times 10^{-15}\text{J}$$

$$t_d = 0.69(30 \times 10^3 \times 1 \times 10^{-15}) = 2.07 \times 10^{-11}\text{s}$$

g) **Compare the energy and delay of process A and B.**

Solution

Compared to process B, process A dissipates less energy per transition, but has a longer delay time.

h) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to $50\text{k}\Omega$. **Calculate the new delay and energy.**

Solution

$$U_s = (1 \times 10^{-15})2^2 = 4 \times 10^{-15}\text{J}$$

$$t_d = 0.69(50 \times 10^3 \times 1 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

i) Based on your previous answers, **which process should Jerry choose to use? Why?**

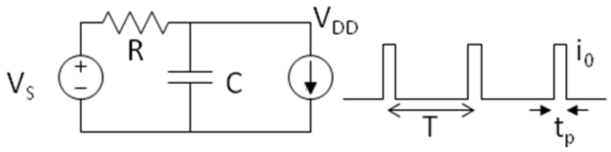
Solution

With the new V_{DD} and R_p of process B, it ends up that process B and process A have the same delay time. However, process B dissipates less energy per transition with the new V_{DD} and R_p, which means Jerry should choose process B which uses the reduced V_{DD}.

5 IC Power Supply

Digital integrated circuits (ICs) often have very non-uniform current requirements which can cause voltage noise on the supply lines. If one IC is adding a lot of noise to the supply line, it can affect the performance of other ICs that use the same power supply, which can hinder performance of the entire device. For this reason, it is important to take measures to mitigate, or "smooth out", the power supply noise that each IC creates. A common way of doing this is to add a "supply capacitor" between each IC and the power supply. (If you look at a circuit board, and the supply capacitor is the small capacitor next to each IC.)

Here's a simple model for a power supply and digital circuit:



The current source is modeling the "spiky," non-uniform nature of digital circuit current consumption. The resistor represents the sum of the source resistance of the supply and any wiring resistance between the supply and the load.

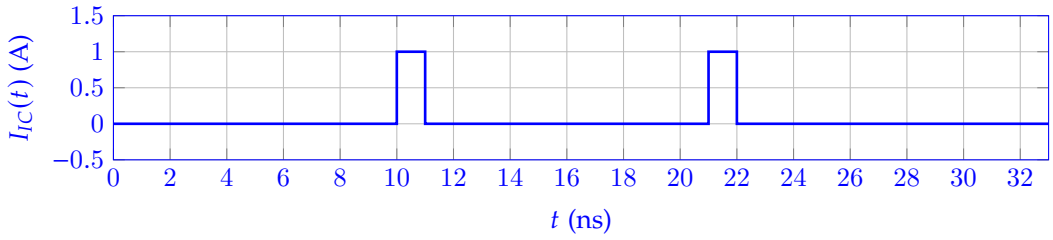
The capacitor is added to try to minimize the noise on V_{DD}. Suppose $V_s = 3$V, $R = 1\Omega$, $i_0 = 1$A, $T = 10$ns, and $t_p = 1$ns. You may also assume that the current has been 0 Amps for a long time prior to anything happening in the circuit.

a) Sketch the voltage V_{DD} vs. time for one or two periods T assuming that $C = 0$.

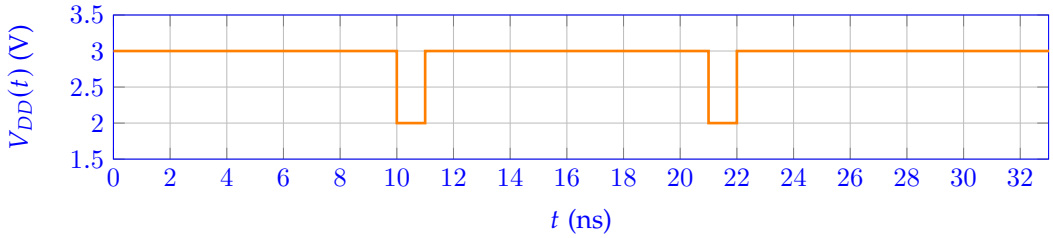
Solution

If $C = 0$, then this circuit will respond instantaneously to changes in the current; thus we may break this down into two segments, wherein the current source $I_{IC}(t)$ equals 0 (and thus $V_{dd} = V_s$), and where the current source $I_{IC}(t)$ equals i_0 (and thus $V_{dd} = V_s - i_0 R = 2$V). These will follow the current source's flips precisely. With that in mind, your sketch should look something like this:

Sketch of transient current drawn by IC



Sketch of transient IC supply voltage



In the above sketch, we have the first current spike at $t = 10$ ns. Yours doesn't have to align with that: for example, if you had the first current spike at $t = 0$, that's okay. However, what *does* matter is that you have the timing between the current spikes drawn correctly.

b) Give expressions for and sketch the voltage V_{DD} vs. time for one or two periods T for each of three different capacitor values for C: 1pF , 1nF, 1μF. (1pF = 10^{-12}F, 1nF = 10^{-9}F, 1μF = 10^{-6}F)

Solution

Since the current through the source is a series of pulses, it will be easiest if we solve for $V_{dd}(t)$ for the two phases if $I_C(t)$.

Starting with KVL:

$$V_s = V_R + V_{dd} \tag{29}$$

$$V_s = (I_C + C\frac{d}{dt}V_{dd})R + V_{dd} \tag{30}$$

$$\frac{d}{dt}V_{dd} = \frac{1}{RC}(V_s - RI_C - V_{dd}) \tag{31}$$

Using the solution of the differential equation $\frac{d}{dt}x(t) + \alpha x(t) = \beta$ seen in lecture,

$$x(t) = x_0 e^{-\alpha t} + \frac{\beta}{\alpha}(1 - e^{-\alpha t})$$

Initially, when $I_C(t) = 0$, and $V_{dd}(0) = V_s$,

$$V_{dd}(t) = V_s e^{-\frac{1}{RC}t} + V_s(1 - e^{-\frac{1}{RC}t}) = V_s$$

Things get exciting once the first current pulse starts such that $I_C = i_0$. The initial condition for this piecewise section is the final voltage V_{dd} from the previous section, V_s. Therefore, since we had the differential equation and $I_C = i_0$,

$$\frac{d}{dt}V_{dd} + \frac{1}{RC}V_{dd} = \frac{1}{RC}(V_s - RI_C)$$

The solution to this differential equation will be

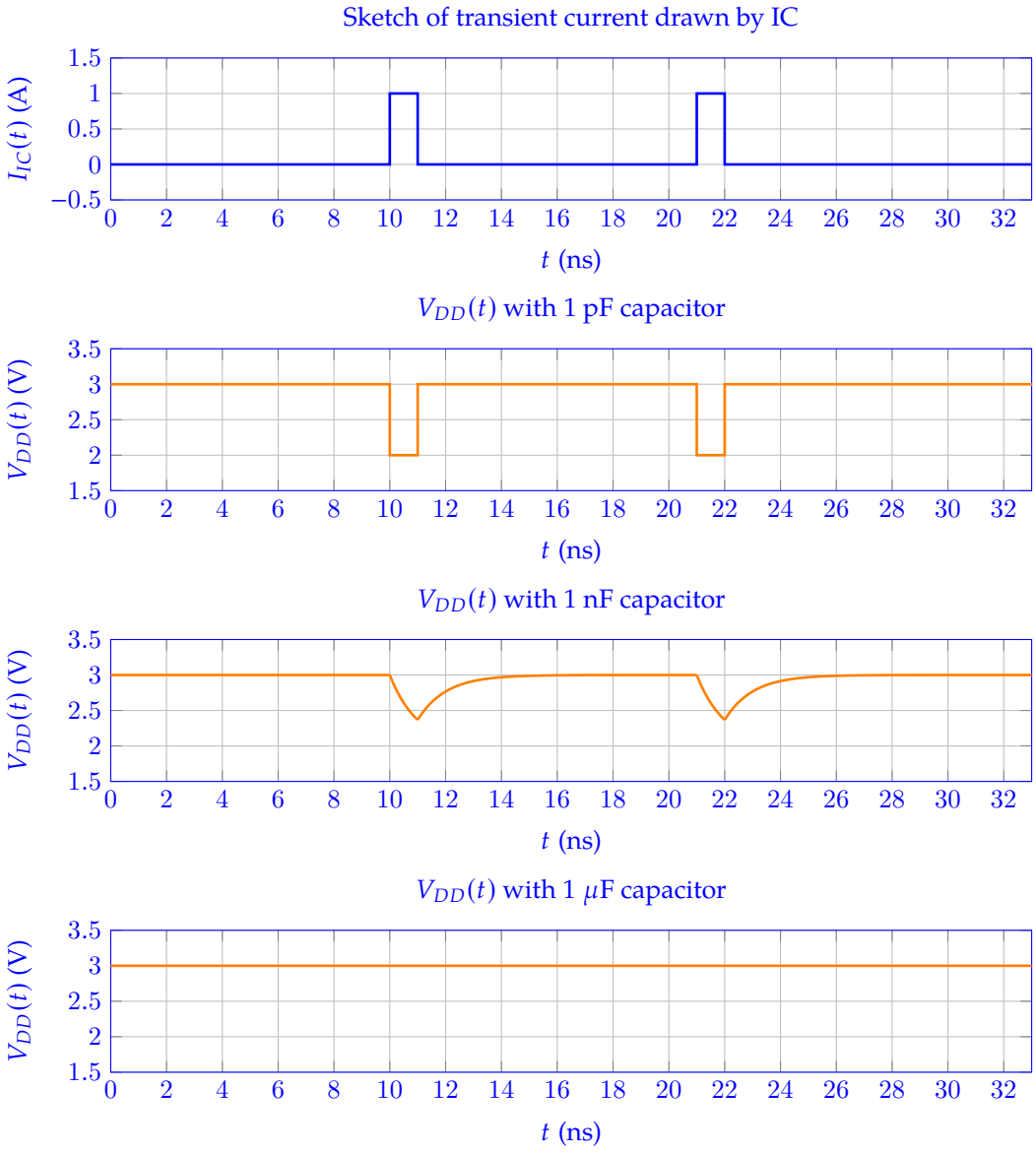
$$V_{dd}(t) = V_s e^{-\frac{1}{RC}t} + (V_s - RI_C)(1 - e^{-\frac{1}{RC}t}) = V_s - RI_C(1 - e^{-\frac{1}{RC}t})$$

You can compute the voltage at the end of the pulse by plugging in $t = t_p$ and the R and C values for your scenario. This voltage will serve as the initial condition for the next piecewise constant section. The process of simplifying the general piecewise differential equation and solving for A can be performed repeatedly to determine the shape of the plot for further pulses.

In general: each of the three curves will tend towards a final value $V_{dd} = V_s$, growing exponentially slower towards this goal as time progresses. However, on each time interval t_p, the current source will start drawing charge from both V_s–whose current decreases as time proceeds–and C–whose charge, and therefore whose potential to contribute voltage, tends to increase with time. With each t_p, V_{dd} decreases nonlinearly, as there are both exponential and linear factors contributing to the rise and fall of the voltage.

With a lower capacitance, we will see the capacitor charge and discharge faster with time–this means that V_{dd} will fluctuate more/change more drastically on t_p; as you increase capacitance, this fluctuation is less evident, as C has more charge to pull from, and will thus be less affected by the change of charge incurred by the current source.

The final sketches should look something like this:



Note that if your solutions contain just the correct plots without much verbose, textual explanation of the plots, then you still deserve full credit.

The idea here is to see the effect that the capacitors have on $V_{DD}(t)$ when viewed at the time scale of the current spikes.

- the 1 pF capacitor causes the RC circuit to have a time constant of $\tau = RC = 1$ps, that is 1picosecond $= 10^{-12}$ seconds, and the effect that this has on $V_{DD}(t)$ is invisible at the nanosecond time scale. For this reason, we can conclude that the 1 pF capacitor would not be adequate to mitigate the noise that the IC will put on the power supply.

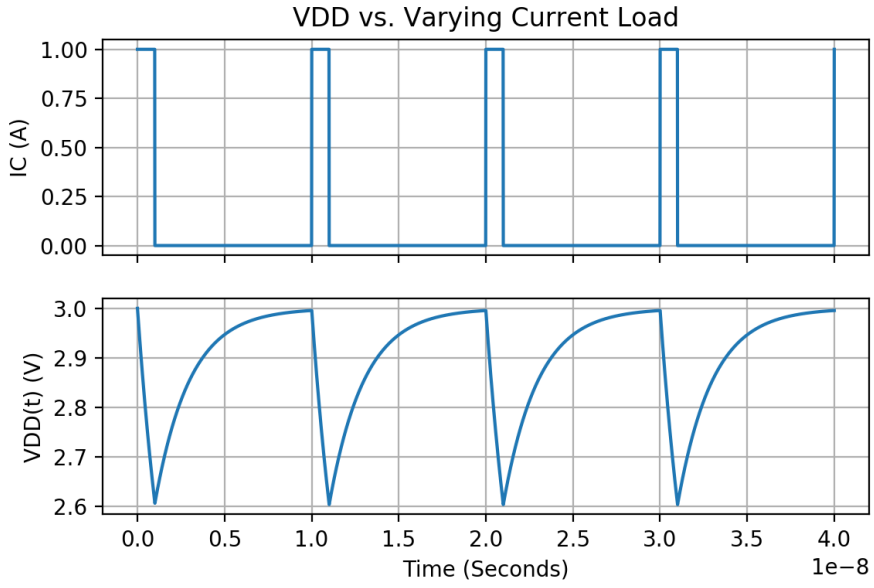
- the 1 nF capacitor causes the RC circuit to have a time constant of $\tau = RC = 1$ns. This is a long enough time scale that the effect on $V_{DD}(t)$ will be visible. At the end of the 1 ns current spike, $V_{DD}(t)$ will have dropped from 3 V to $2+\exp(-1) \approx 2.37$ V. This means that the 1 nF capacitor is actually reducing the power supply noise a little bit, but not much.
- the 1 μF capacitor causes the RC circuit to have a time constant of $\tau = RC = 1\mu$s. This time constant is 1000 times longer than the duration of the current spike. At the end of the current spike, $V_{DD}(t)$ will have dropped by only one millivolt, so at the scale at which these sketches are drawn, there is no visible change. The 1 μF capacitor has almost totally removed the power supply noise.

c) Launch the attached Jupyter notebook to interact with a simulated version of this IC power supply. Try to simulate the scenarios outlined in the previous parts. For one of these scenarios, keep the RC time constant fixed, but vary the relative value of R vs. C (e.g. compare $R = 1, C = 2e-9$ to the case where $R = 2, C = 1e-9$). **Is it better to have a lower R or lower C value for a fixed RC time constant when attempting to minimize supply noise? Give an intuitive explanation for why this might be the case.**

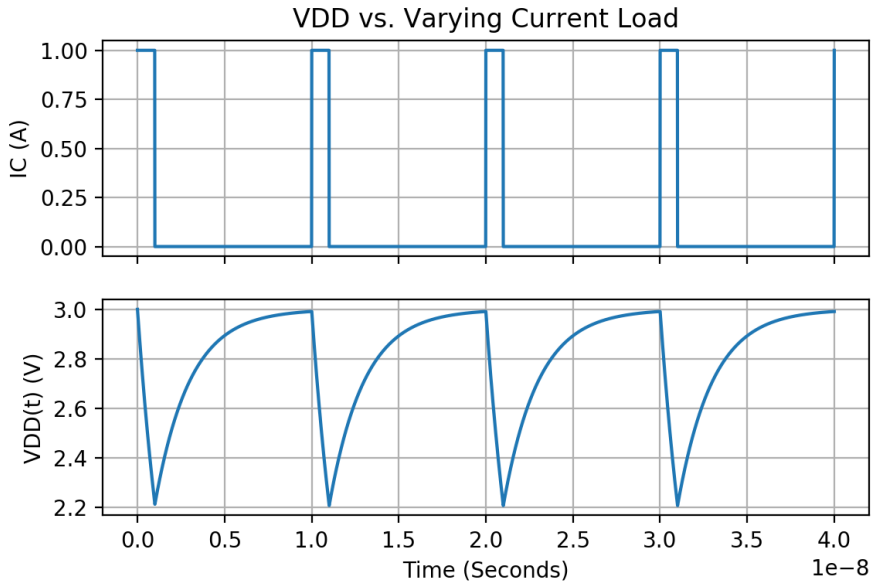
Solution

A lower resistance and higher capacitance leads to smaller variation in the supply voltage with each current spike. One intuitive way to see this is to think about where the charge comes from whenenver the current source turns on. The charge comes from the capacitor and from the voltage source through the resistor. By $Q = CV$ for a constant amount of charge drawn, a larger capacitor results in lower voltage change. By $V = IR$ for a constant amount of current drawn through the resistor, a larger resistor leads to a larger voltage drop.

In the case where $R = 1$ and $C = 2e-9$, we get the following plot:



In the case where $R = 2$ and $C = 1e - 9$, we get the following plot:



Notice that the shape of the V_{dd} curves is the same becuase the RC constant is the same. However they drop to different voltages by the end of each pulse.

6 Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student! We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

a) **What sources (if any) did you use as you worked through the homework?**

b) **How did you work on this homework?** (For example, *I first worked by myself for 2 hours, but got stuck on problem 3, so I went to office hours. Then I went to homework party for a few hours, where I finished the homework.*)

c) Use the provided course resources (Piazza, Meet Event, Random Assignment) to create your study group (min 3 people) this week. This will be your study group to meet with or ignore as much as you please. Although you are always free to collaborate with other people, make sure everyone is on the same page about how they want to use the study group. Your study group does not have to be your lab group. **Lastly, take a screenshot of everyone in a group chat (zoom call, slack channel, etc.)**

d) **Write down your plans for how you want to use the study group (to get points on this problem, memes, and homework help are all valid).**

e) **Do you have any feedback on this homework assignment?**

f) **Roughly how many total hours did you work on this homework?**