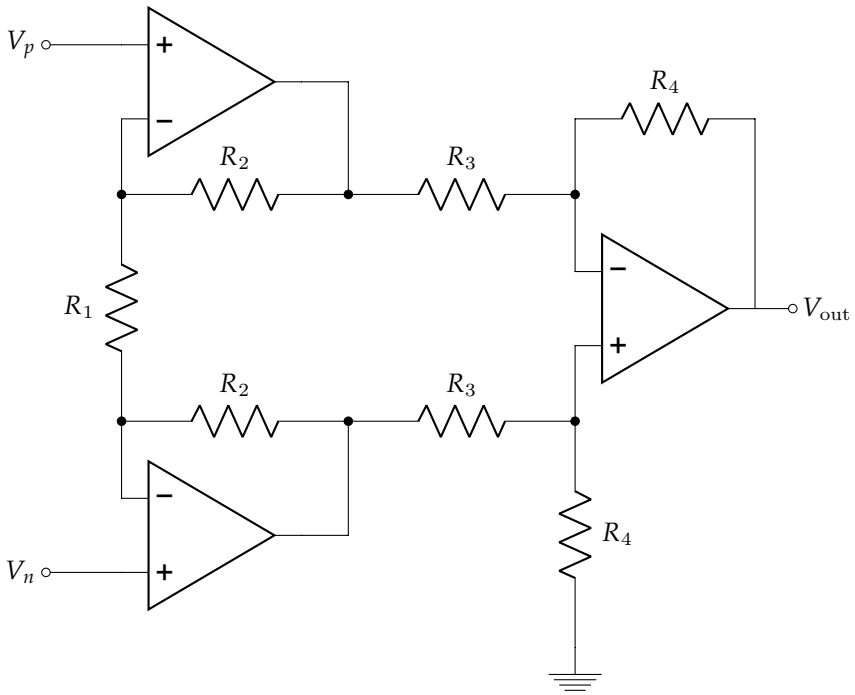
This homework is due on Tuesday, June 30, 2020, at 11:59PM.
Self-grades are due on Tuesday, July 7, 2020, at 11:59PM.

1 Op-Amp Review

Consider the circuit below:



a) Write down all branch and node equations using KCL and the Golden Rules of op-amps.

b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two R_2's? How do the currents of R_2's influence the current through R_1?

c) What is the current through R_1?

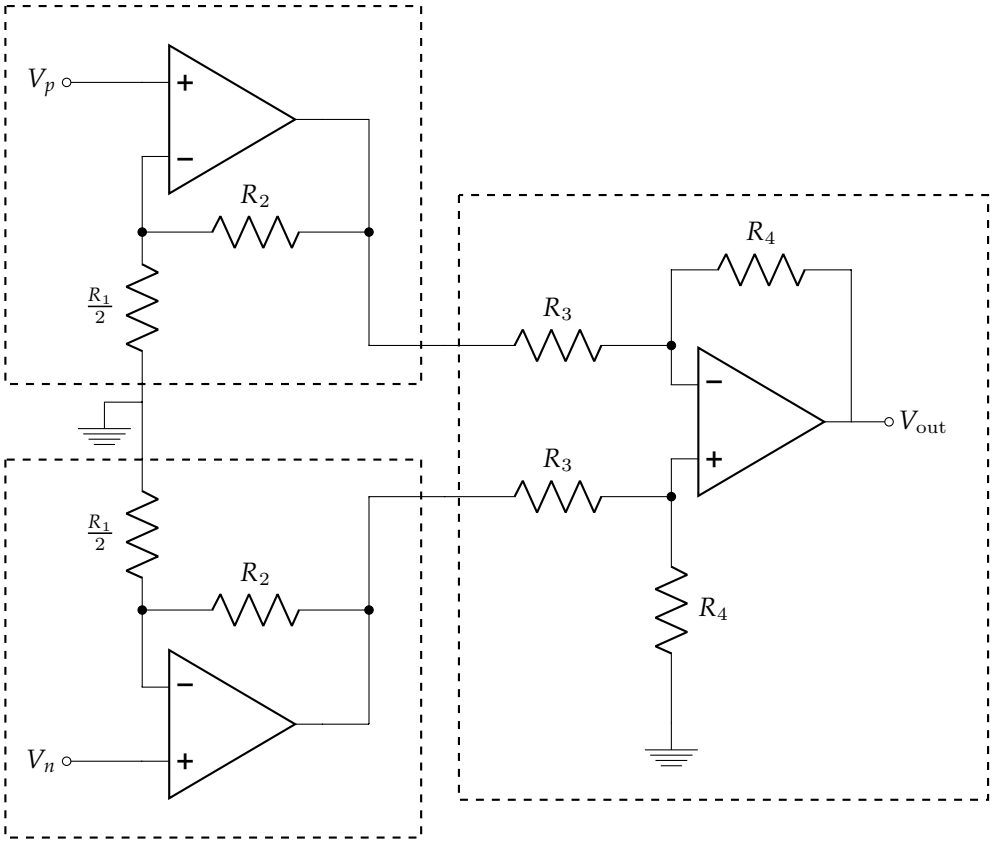
d) What are the output voltages of the two op-amps at the first stage?

e) Compute the voltage at the + terminal of the second-stage op-amp.

f) What is V_{out}?

g) If we broke R_1 into two series resistors, each with a resistance of $\frac{R_1}{2}$, what is the voltage at the node in between these resistors?

h) Based on the above analysis, if $V_p = -V_n$, we could introduce a "fake ground" in the middle of the resistor R_1 and come up with the following circuit:



Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks?

What is $\frac{V_{\text{out}}}{V_p - V_n}$ for this revised circuit?

2 Existence and uniqueness of solutions to differential equations

Let's show that if any function x satisfies

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \alpha x(t) \tag{1}$$

as well as

$$x(0) = x_0, \tag{2}$$

then it is unique: if y is *any function* that meets these two criteria then $x = y$.

In order to do this, we will first verify that a solution exists. Then we will compare it to a hypothetical alternative solution—and our goal will to be establish that these two solutions are equal.

a) **Verify that $x_d(t) = x_0 e^{\alpha t}$ satisfies** (1) **and** (2)**.** (For this proof, x_d will be the "reference solution" against which alternates will be compared.)

b) To show that this solution is in fact unique, we need to consider a hypothetical $y(t)$ that also satisfies (1) and (2).

Our goal is to show that $y(t) = x(t)$ for all $t \geq 0$. (The domain $t \geq 0$ is where we have defined the conditions (1) and (2). Outside of that domain, we don't have any constraints.)

How can we show that two things are equal? In the past, you have probably shown that two quantities or functions are equal by starting with one of them, and then manipulating the expression for it using valid substitutions and simplifications until you get the expression for the other one. However, here, we don't have an expression for $y(t)$ so that style of approach won't work.

In such cases, we basically have a couple of basic ways of showing that two things are the same.

- Take the difference of them, and somehow argue that it is 0.
- Take the ratio of them, and somehow argue that it is 1.

We will follow the ratio approach in this problem. First assume that $x_0 \neq 0$. In this case, we are free to define $z(t) = \frac{y(t)}{x_d(t)}$ since we are dividing by something other than zero.

What is $z(0)$?

c) **Take the derivative $\frac{d}{dt}z(t)$ and simplify using** (1) **and what you know about the derivative of $x_d(t)$.**

(HINT: The quotient rule for differentiation might be helpful since a ratio is involved.)

You should see that this derivative is always 0 and hence $z(t)$ does not change. **What does that imply for y and x_d ?**

d) At this point, we have shown uniqueness in most cases. Just one special case is left: $x_0 = 0$. The ratio technique omitted this case, because as $x_d(t) = 0$, x_d cannot be the denominator of a fraction.

To complete our proof we must to show that if $x_0 = 0$, then $y(t) = 0$ for all t, and we will do so by assuming that $y(t)$ is not identically 0 for $t > 0$—that is, at some $t_0 > 0$ $y(t_0) = k \neq 0$.

From (2), we know that $y(0) = 0$. In this part, we will try to work backwards in time from the point $t = t_0$ to $t = 0$ and conclude that y violates (2).

Apply the change of variables $t = t_0 - \tau$ to (1) to get a new differential equation for $\widetilde{x}(\tau) = x(t_0 - \tau)$ that specifies how $\frac{d}{d\tau}\widetilde{x}(\tau)$ must relate to $\widetilde{x}(\tau)$. This should hold for $-\infty < \tau \leq t_0$.

e) Because the previous part resulted in a differential equation of a form for which we have already proved uniqueness for the case of nonzero initial condition, and since $\widetilde{y}(0) = y(t_0) = k \neq 0$, we know what $\widetilde{y}(\tau)$ must be. **Write the expressions for $\widetilde{y}(\tau)$ for $\tau \in [0, t_0]$ and what that implies for $y(t)$ for $t \in [0, t_0]$.**

f) **Evaluate $y(0)$ and argue that this is a contradiction for the specified initial condition** (2).

Consequently, such a $y(t)$ cannot exist and only the all zero solution is permitted — establishing uniqueness in this case of $x_0 = 0$ as well.

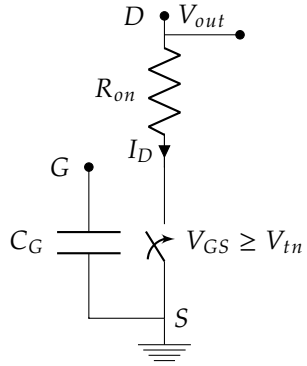
g) Explain in your own words why it matters that solutions to these differential equations are unique.

Although we gave you lots of guidance in this problem, we hope that you can internalize this way of thinking.

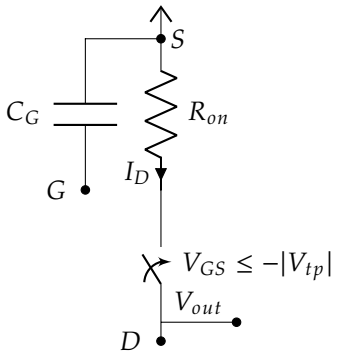
This elementary approach to proving the uniqueness of solutions to differential equations works for the kinds of linear differential equations that we will tend to encounter in EE16B. For more complicated nonlinear differential equations, further conditions are required for uniqueness (appropriate continuity and differentiability) and proofs can be found in upper-division mathematics courses on differential equations when you study the Picard-Lindelöf theorem. (It involves looking at the magnitude of the difference of the two hypothetical solutions and showing this has to be arbitrarily small and hence zero. However, the basic elementary case we have established here can be viewed as a building block — the quotient rule gets invoked in the appropriate place, etc. The additional ingredients that are out-of-scope for lower-division courses are fixed-point theorems — which you can think of as more general siblings of the intermediate-value theorem you saw in basic calculus.)

3 Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitance C_G represents the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model



(b) PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_G = 1\text{fF}$ (femto-Farads = 10^{-15}). We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e. , the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (fig. 2).

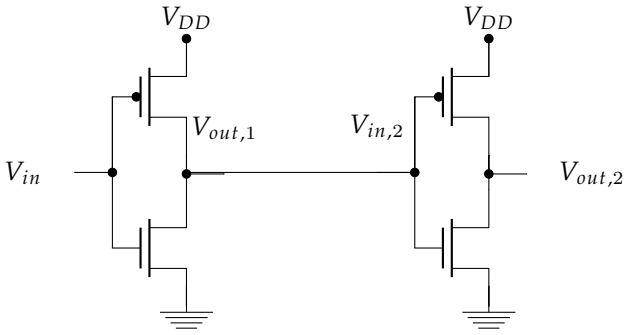


Figure 2: CMOS Inverter chain

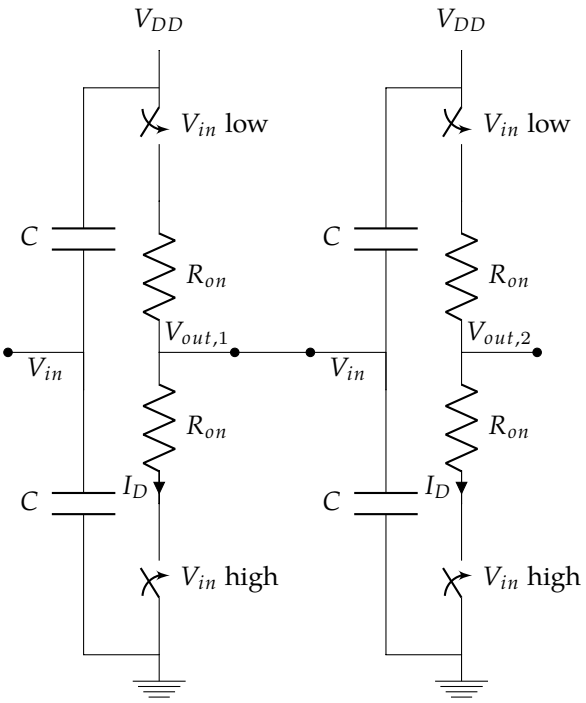


Figure 3: Inverter Transistor Resistor-switch model

a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,1}$) for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

b) Given the initial conditions in part (a), **solve for $V_{out,1}(t)$.**

c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

d) A long time later, the input to the first inverter switches low again.
Solve for $V_{out,1}(t)$.
Sketch the output voltage of the first inverter ($V_{out,1}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.

4 CMOS Scaling

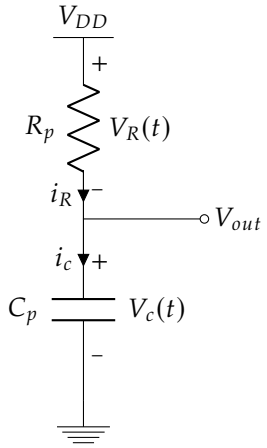
Jerry wants to create a new machine learning accelerator chip using CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transitions and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate). These two parameters are very important for CMOS technology, as they determine how quickly the processor can run and how much power it will consume.

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1\text{V}$. The transistors have a parasitic resistance of $R_p = 10\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5\text{fF}$.

Process B uses a supply voltage of $V_{DD} = 3\text{V}$. The transistors have a parasitic resistance of $R_p = 30\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1\text{fF}$.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:



Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

a) In terms of the variables V_{DD}, R_p, and C_p, **solve for** $V_{out}(t)$.

b) Using the expression for $V_{out}(t)$ that was just calculated, **solve for** $i_R(t)$. Keep this expression in terms of the variables V_{DD}, R_p, and C_p.

c) In the previous part, you should have noticed that $i_R(t)$ started at some value, and decayed towards 0 as $t \to \infty$.

Why does this trend make sense? If the voltage were switching to a different level, would the same trend in current hold? This question is meant to help build intuition and understanding about switching circuits.

d) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the time it takes for** V_{out} **to reach** $\frac{V_{DD}}{2}$.

e) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}.**

For this problem, recall that the instantaneous power delivered by a voltage source is $P(t) = I(t) \cdot V(t)$. Note that the current and voltage are functions of time.

Energy can be found by integrating power:

$$E = \int_{t=0}^{t=\infty} P(t)dt$$

Remember that the units of energy are Joules [J], while the units of power are Watts [W], which is energy per time: $1\text{W} = \frac{1\text{J}}{1\text{s}}$

f) **Repeat parts (d) and (e), but with the values from process B.**

g) **Compare the energy and delay of process A and B.**

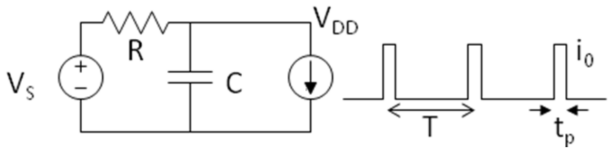
h) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to $50\text{k}\Omega$. **Calculate the new delay and energy.**

i) Based on your previous answers, **which process should Jerry choose to use? Why?**

5 IC Power Supply

Digital integrated circuits (ICs) often have very non-uniform current requirements which can cause voltage noise on the supply lines. If one IC is adding a lot of noise to the supply line, it can affect the performance of other ICs that use the same power supply, which can hinder performance of the entire device. For this reason, it is important to take measures to mitigate, or "smooth out", the power supply noise that each IC creates. A common way of doing this is to add a "supply capacitor" between each IC and the power supply. (If you look at a circuit board, and the supply capacitor is the small capacitor next to each IC.)

Here's a simple model for a power supply and digital circuit:



The current source is modeling the "spiky," non-uniform nature of digital circuit current consumption. The resistor represents the sum of the source resistance of the supply and any wiring resistance between the supply and the load.

The capacitor is added to try to minimize the noise on V_{DD}. Suppose $V_s = 3$V, $R = 1\Omega$, $i_0 = 1$A, $T = 10$ns, and $t_p = 1$ns. You may also assume that the current has been 0 Amps for a long time prior to anything happening in the circuit.

a) Sketch the voltage V_{DD} vs. time for one or two periods T assuming that $C = 0$.

b) Give expressions for and sketch the voltage V_{DD} vs. time for one or two periods T for each of three different capacitor values for C: 1pF , 1nF, 1μF. (1pF = 10^{-12}F, 1nF = 10^{-9}F, 1μF = 10^{-6}F)

c) Launch the attached Jupyter notebook to interact with a simulated version of this IC power supply. Try to simulate the scenarios outlined in the previous parts. For one of these scenarios, keep the RC time constant fixed, but vary the relative value of R vs. C (e.g. compare $R = 1, C = 2e-9$ to the case where $R = 2, C = 1e-9$). **Is it better to have a lower R or lower C value for a fixed RC time constant when attempting to minimize supply noise? Give an intuitive explanation for why this might be the case.**

6 Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student! We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

a) **What sources (if any) did you use as you worked through the homework?**

b) **How did you work on this homework?** (For example, *I first worked by myself for 2 hours, but got stuck on problem 3, so I went to office hours. Then I went to homework party for a few hours, where I finished the homework.*)

c) Use the provided course resources (Piazza, Meet Event, Random Assignment) to create your study group (min 3 people) this week. This will be your study group to meet with or ignore as much as you please. Although you are always free to collaborate with other people, make sure everyone is on the same page about how they want to use the study group. Your study group does not have to be your lab group. **Lastly, take a screenshot of everyone in a group chat (zoom call, slack channel, etc.)**

d) **Write down your plans for how you want to use the study group (to get points on this problem, memes, and homework help are all valid).**

e) **Do you have any feedback on this homework assignment?**

f) **Roughly how many total hours did you work on this homework?**