1 Transistor Introduction

Transistors (as presented in this course) are 3 terminal, voltage controlled switches. This means that, when a transistor is "on," it connects the Source (S) and Drain (D) terminals via a low resistance path (short circuit). When a transistor is "off," the Source and Drain terminals are disconnected (open circuit).

Two common types of transistors are NMOS and PMOS transistors. Their states (shorted or open) are determined by the voltage difference across the Gate (G) and Source (S) terminals, compared to a "threshold voltage." Transistors are extremely useful in digital logic design since we can implement Boolean logic operators using switches.

Recall that in this class, V_{tn} denotes how much **higher** the gate needs to be relative to the source for the NMOS to be on, and that $|V_{tp}|$ denotes how much **lower** the gate needs to be relative to the source for the PMOS to be on.

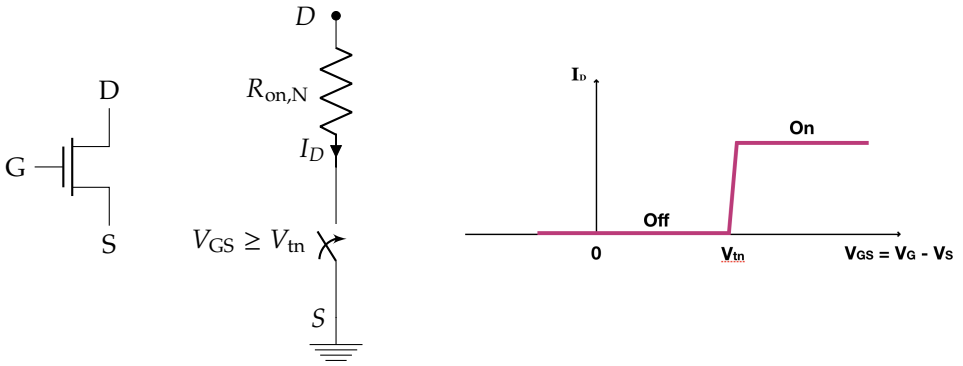

Figure 1: NMOS Transistor Resistor-switch model

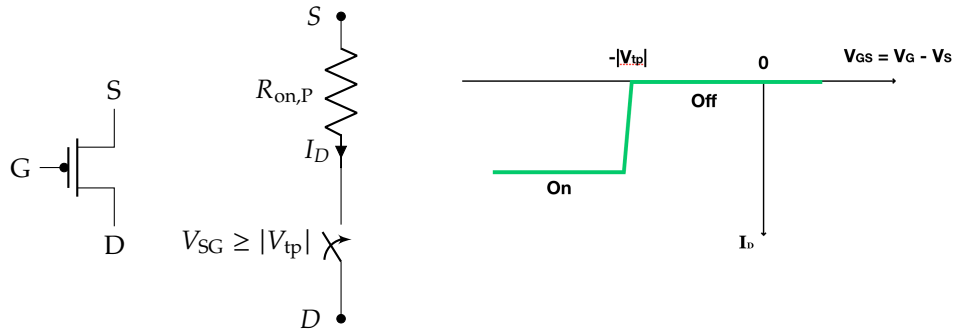

Figure 2: PMOS Transistor Resistor-switch model

Transistors can be connected together to perform boolean algebra. For example, the following circuit is called an "inverter" and represents a NOT gate.

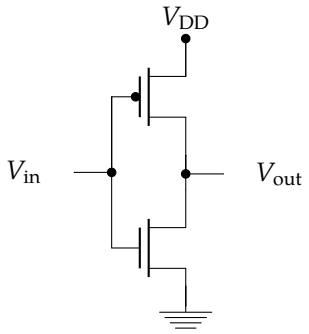

Figure 3: CMOS Inverter

When the input is high ($V_{in} \geq V_{tn}$, $V_{in} \geq V_{DD} - |V_{tp}|$), then the NMOS transistor is on, the PMOS transistor is off, and $V_{out} = 0$. When the input is low ($V_{in} \leq V_{tn}$, $V_{in} \leq V_{DD} - |V_{tp}|$), the NMOS transistor is off, the PMOS transistor is on, and $V_{out} = V_{DD}$. When working with digital circuits like the one above, we usually only consider the values of $V_{in} = 0, V_{DD}$. This yields the following truth table:

V_{in}	V_{out}	NMOS	PMOS
V_{DD}	0	on	off
0	V_{DD}	off	on

If you think of V_{DD} being a logical 1 and $0\,\text{V}$ being a logical 0, we have just created the most elementary logical operation using transistors!

2 Single-transistor Inverter

Consider the following single-transitor inverter, consisting of an NMOS transistor and a resistor, where for N_1 we have $0 < V_{tn} < V_{DD}$.

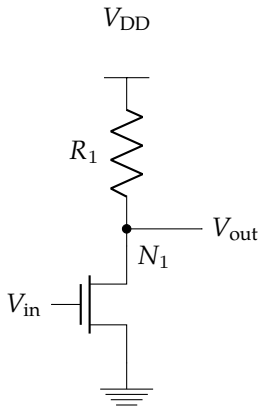

Figure 4: Single transistor NMOS inverter

a) Replace the transistor N_1 with a switch, the simplest model of a transistor and answer the following questions

   (i) What is V_{out} when $V_{\text{in}} = 0$?

   (ii) What is V_{out} when $V_{\text{in}} = V_{\text{DD}}$?

   (iii) What is the power consumption of the circuit when $V_{\text{in}} = 0$? How about when $V_{\text{in}} = V_{\text{DD}}$

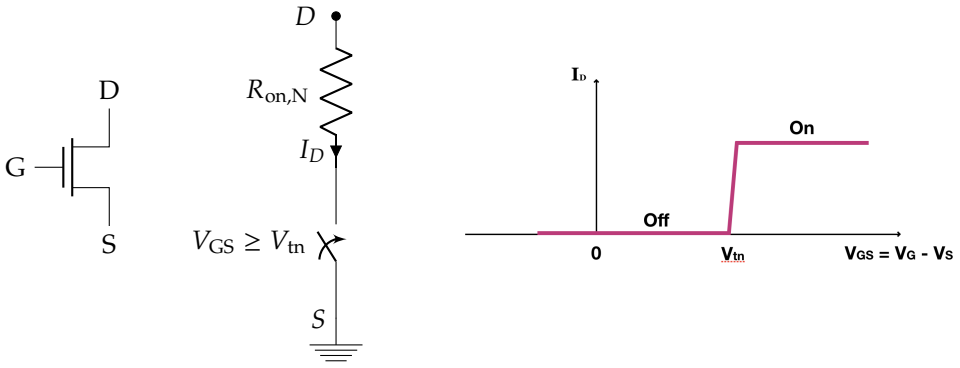

Figure 5: NMOS Transistor Resistor-switch model

b) Now replace the NMOS device with a transistor model that includes an internal resistor, such as the one in the figure above.

(i) What is V_{out} when $V_{in} = 0$?

(ii) What is V_{out} when $V_{in} = V_{DD}$ in terms of R_1 and $R_{on,\,N}$?
What is this value if $R_{on,N} = \frac{1}{10}R_1$?
How much power does the circuit consume?

c) Now consider a CMOS inverter with both PMOS and CMOS devices, such as that of Figure 3. How does the performance and power consumption compare?

3 NAND Circuit

Let us consider a NAND logic gate. This circuit implements the boolean function $\overline{(A \cdot B)}$.

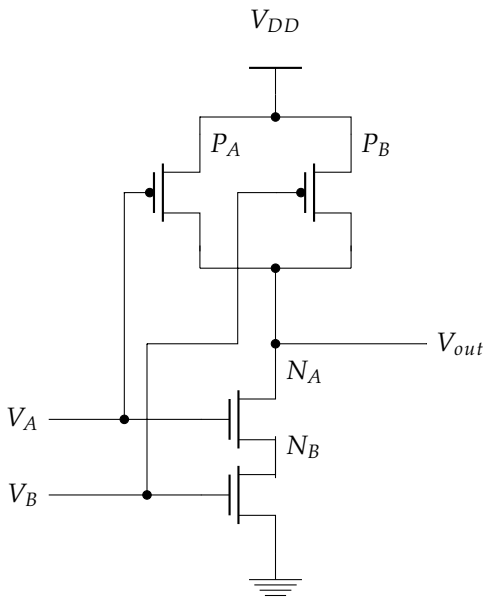

Figure 6: NAND

V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

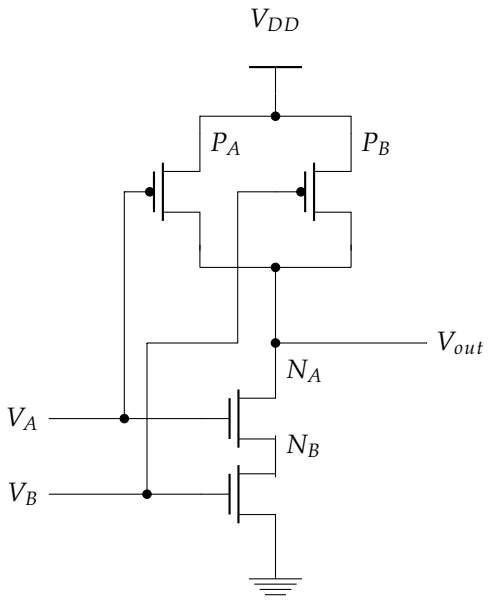

Figure 7: NAND

b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open circuits? Which transistors act like closed circuits? What is V_{out}?

c) If $V_A = 0V$ and $V_B = V_{DD}$, what is V_{out}?

d) If $V_A = V_{DD}$ and $V_B = 0V$, what is V_{out}?

e) If $V_A = 0V$ and $V_B = 0V$, what is V_{out}?