EECS 16B Designing Information Systems and Devices II UC Berkeley Spring 2022

Homework 1

This homework is due on Friday, January 28, 2022, at 11:59PM. Self-grades and HW Resubmissions are due on the following Friday, February 4, 2022, at 11:59PM.

1. **Group Formation Survey**

   Please fill out this group formation survey if you are interested in getting matched up in a study group. We highly recommend joining a study group in order to foster a sense of community in the course and learn from others. EECS 16B is a pretty fast-paced course, and you can benefit quite a bit from your peers' perspectives on the material.

   Within a few weeks, you should get an email informing you of the group you have been matched with. It is respectful and professional behavior to follow up with your group members; completing this survey suggests you are interested in joining a group, after all – we hope you stay true to your word!

   Special shoutout to Prof. Ranade's group formation research team for making this possible!

   Just so you have an answer to put down for this question, write down whether you filled out the survey or not.

   Solution: Any answer is fine and merits full points.

2. Reading Lecture Notes

Staying up to date with lectures is an important part of the learning process in this course. Here are links to the notes that you need to read for this week: Note j, Note 1

(a) **Have you seen the vector representation of complex numbers in Note j before?** Question 3 explores the topics in more details.

Solution: Any answer is acceptable. The important thing here is having read the note.

(b) **Have you solved differential equations of this form before?**

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \alpha x(t) \tag{1}$$

Questions 6 and 7 explore the topics of Note 1 in more details.

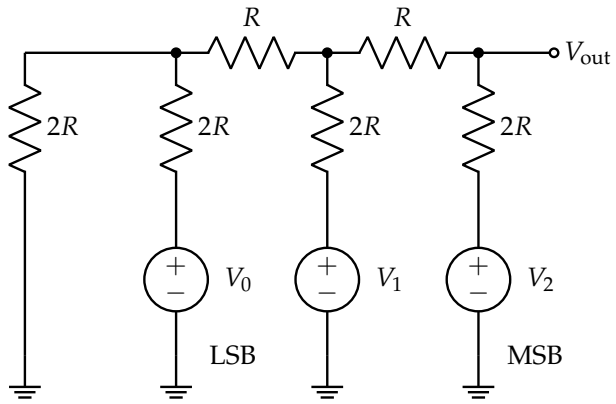
Solution: Any answer is acceptable. The important thing here is having read the note.

These kinds of differential equations are nominally in scope for Math 1B but are sometimes just covered as a teaser instead of having students do lots of problems, etc.

3. Digital-Analog Converter

A digital-analog converter (DAC) is one of the key interface components between the digital and the analog world. It is a circuit for converting a digital representation of a number (binary) into a corresponding analog voltage. In this problem, we will consider a DAC made out of resistors only (resistive DAC) called the R-$2R$ ladder. This DAC will help us generate the analog voltages from the digital representation, and later will also help us digitize the analog voltages when we will be building analog to digital interfaces in Lab 3, in part based on this ladder-DAC.

Here is the circuit for a 3-bit resistive DAC.

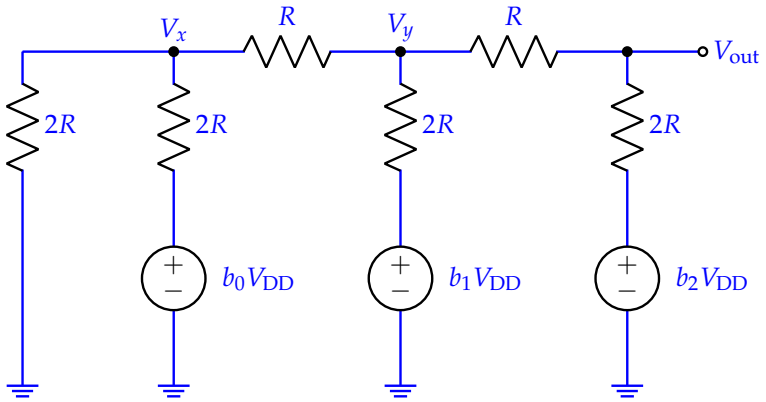


Let $b_0, b_1, b_2 = \{0, 1\}$ (that is, either 1 or 0), and let the voltage sources $V_0 = b_0 V_{DD}$, $V_1 = b_1 V_{DD}$, $V_2 = b_2 V_{DD}$, where V_{DD} is the supply voltage.

As you may have noticed, (b_2, b_1, b_0) represents a 3-bit binary (unsigned) number where each of b_i is a binary bit. b_0 is the least significant bit (LSB) and b_2 is the most significant bit (MSB). We will now analyze how this converter functions.

(a) **Solve for V_{out} in terms of V_{DD} and the binary bits b_2, b_1, b_0.**

Solution: There are several ways to solve this problem. The first way is to use KCL and create a system of equations which we solve for using Gaussian elimination.



Applying KCL at nodes V_x, V_y, and V_{out} and substituting in for the currents through the resistors, we get

$$\frac{V_x}{2R} + \frac{V_x - b_0 V_{DD}}{2R} + \frac{V_x - V_y}{R} = 0 \tag{2}$$

$$\frac{V_y - b_1 V_{DD}}{2R} + \frac{V_y - V_x}{R} + \frac{V_y - V_{out}}{R} = 0 \tag{3}$$

$$\frac{V_{\text{out}} - b_2 V_{\text{DD}}}{2R} + \frac{V_{\text{out}} - V_y}{R} = 0 \tag{4}$$

This system of equations can be solved using substitution or Gaussian elimination. One approach is shown below:
Multiplying (2), (3), (4) by R, we get

$$2V_x - \frac{b_0 V_{\text{DD}}}{2} - V_y = 0 \tag{5}$$

$$\frac{5V_y}{2} - \frac{b_1 V_{\text{DD}}}{2} - V_x - V_{\text{out}} = 0 \tag{6}$$

$$\frac{3V_{\text{out}}}{2} - \frac{b_2 V_{\text{DD}}}{2} - V_y = 0 \tag{7}$$

Adding $\frac{1}{4}\times$ (5), $\frac{1}{2}\times$ (6), and (7), we get

$$V_{\text{out}} - \frac{b_2 V_{\text{DD}}}{2} - \frac{b_1 V_{\text{DD}}}{4} - \frac{b_0 V_{\text{DD}}}{8} = 0 \tag{8}$$

$$\implies \frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}} \tag{9}$$

Plugging in 1, 0, 0 into (9) gives the answer.

$$V_{\text{out}} = \frac{V_{\text{DD}}}{2} \tag{10}$$

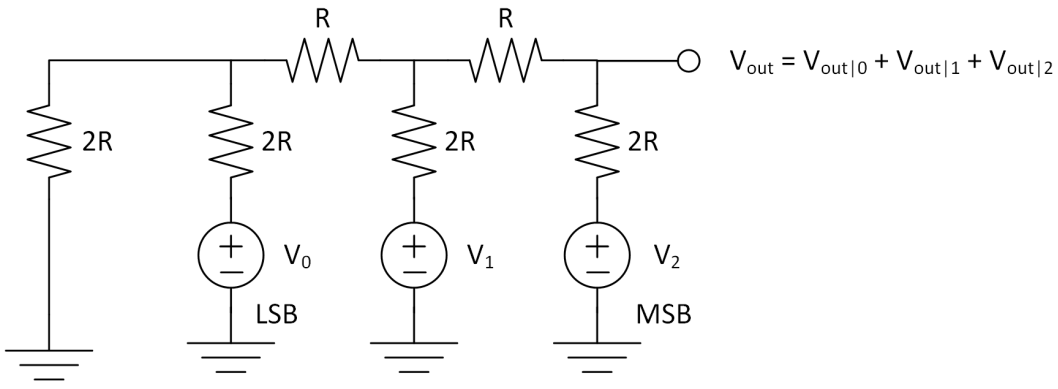
While using KCL and Gaussian elimination is a correct way of solving this problem, there is another way by using superposition and Thevenin equivalent circuits which you learned in EE16A. This approach tends to be more "intuitive": it helps you understand why the circuit was designed the way it was, how to quickly solve for the circuit (in your head, with enough practice), and transfer key design principles to invent new circuits for new problems. These skills are key to a successful career in engineering.

Recall that the output voltage is a superposition of all the independent voltage and current sources in the circuit as seen at the output. In other words, we can turn on each independent source separately, solve for the output voltage for that given source, repeat for each independent source, and sum the output voltages for each case. This will be the final output voltage.

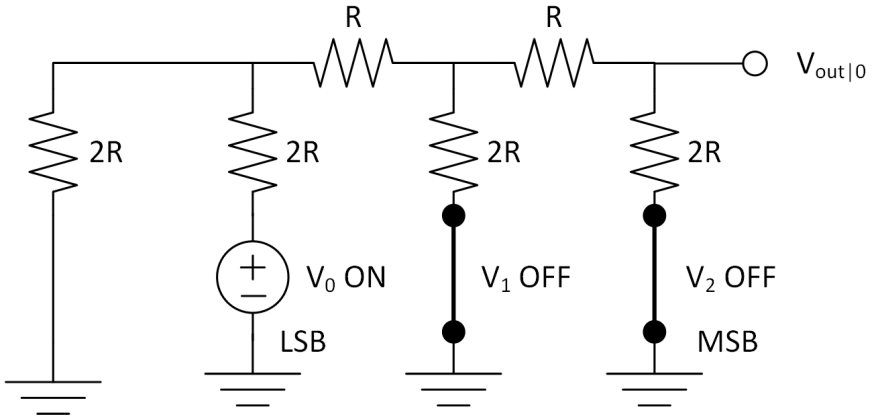
Mathematically, we can write this as:

$$V_{\text{out}} = V_{\text{out}|0} + V_{\text{out}|1} + V_{\text{out}|2} \tag{11}$$

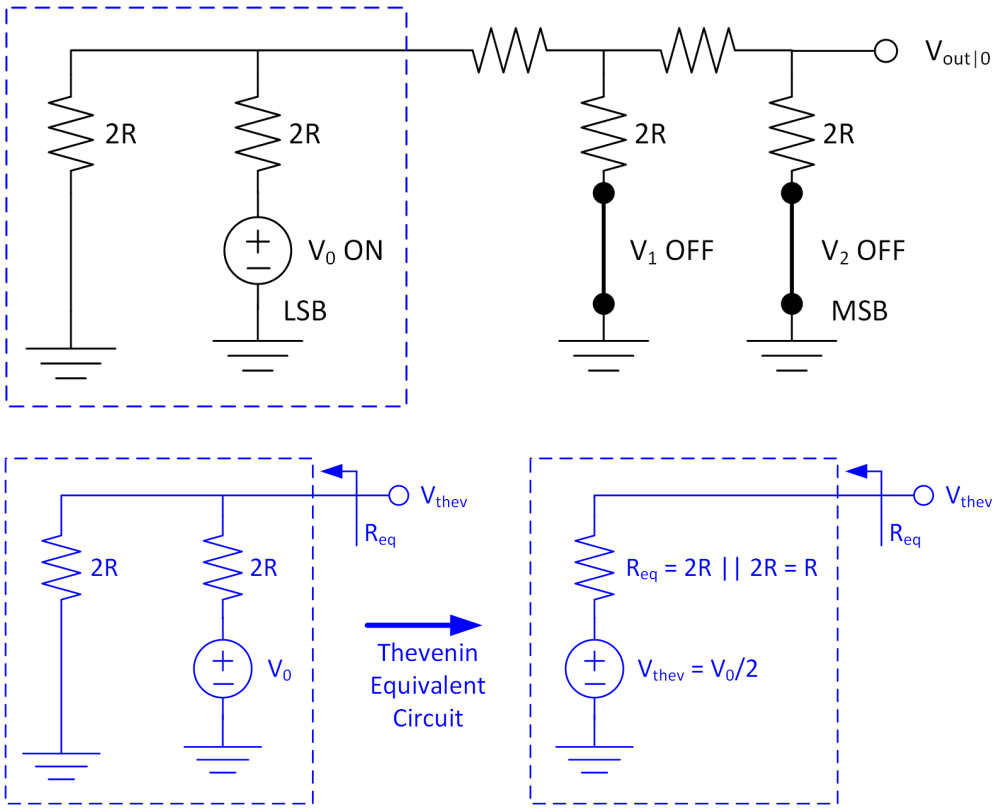
where $V_{\text{out}|0}$ refers to V_{out} due to independent source 0 on and all other sources off.

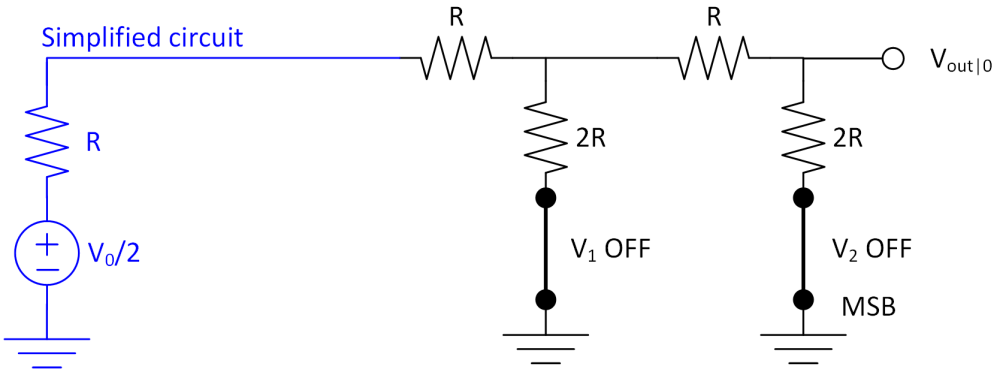


Let's first solve for $V_{out|0}$. To do so, re-draw the circuit with the independent voltage source V_0 on and all the other independent sources, voltage sources V_1 and V_2, off. Recall that when we turn a voltage source off, we treat it as a short circuit, i.e. 0 Volts (as opposed to turning a current source off, which we treat as an open circuit, i.e. 0 Amps). We show this circuit below.

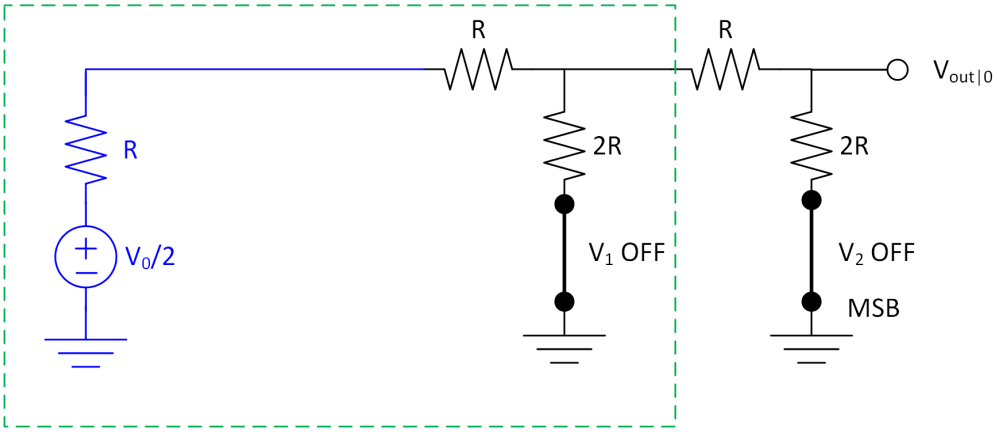


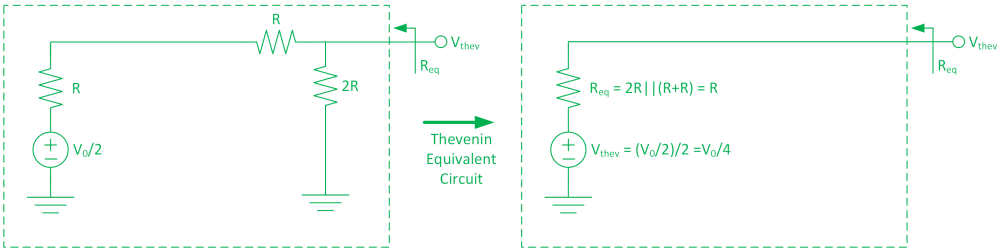
We then want to solve for $V_{out|0}$ by using Thevenin equivalent circuits to simplify the problem. We will conduct Thevenin simplification twice. First, draw a bounding box around the components we want to simplify. How you draw this box depends on how much you want to simplify at once (you get better with practice). We choose to draw the blue dotted box, find the corresponding Thevenin circuit, and replace the original components with their equivalent circuit.

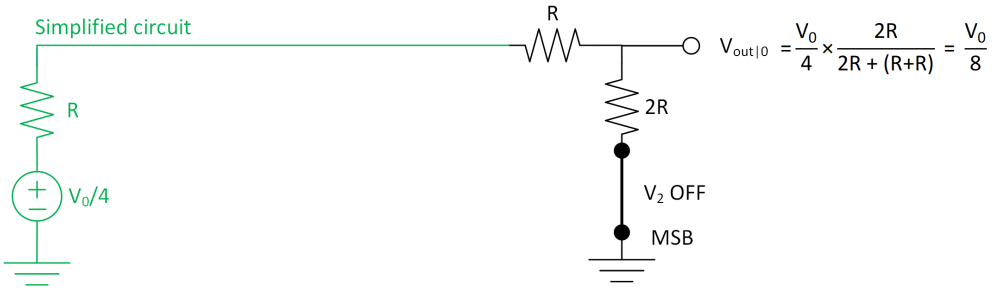




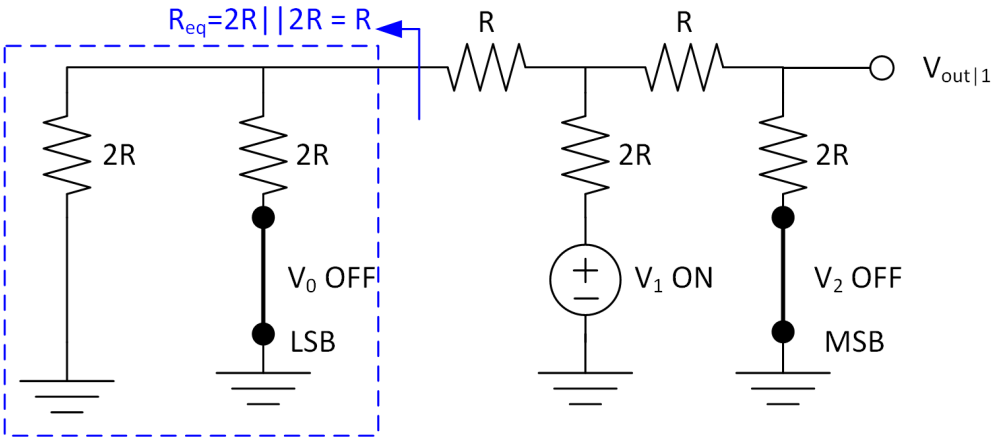
We then conduct a second round of Thevenin using the green dotted box below. From the resulting simplified circuit, we see what's left is a straightforward voltage divider, and solve for $V_{out|0}$ directly.

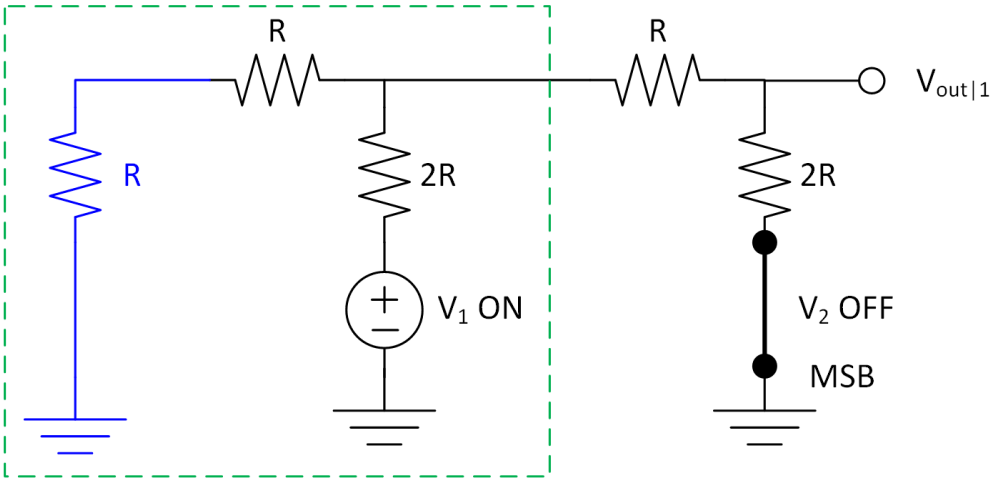


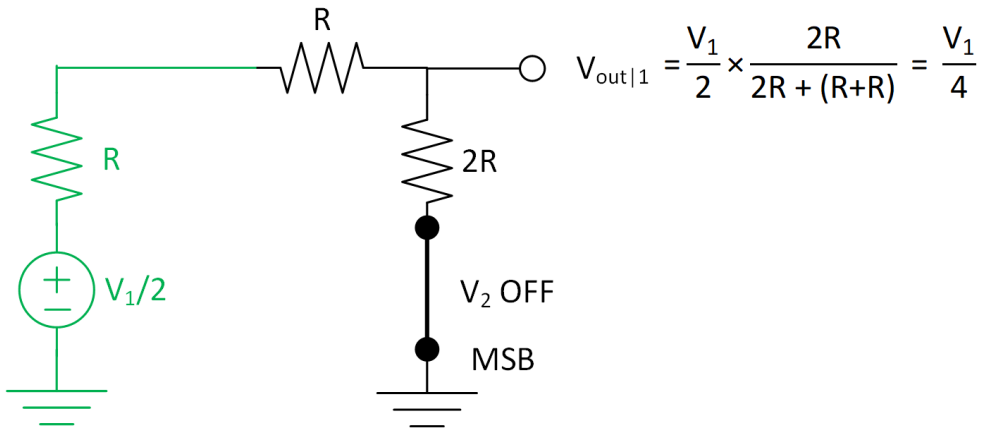




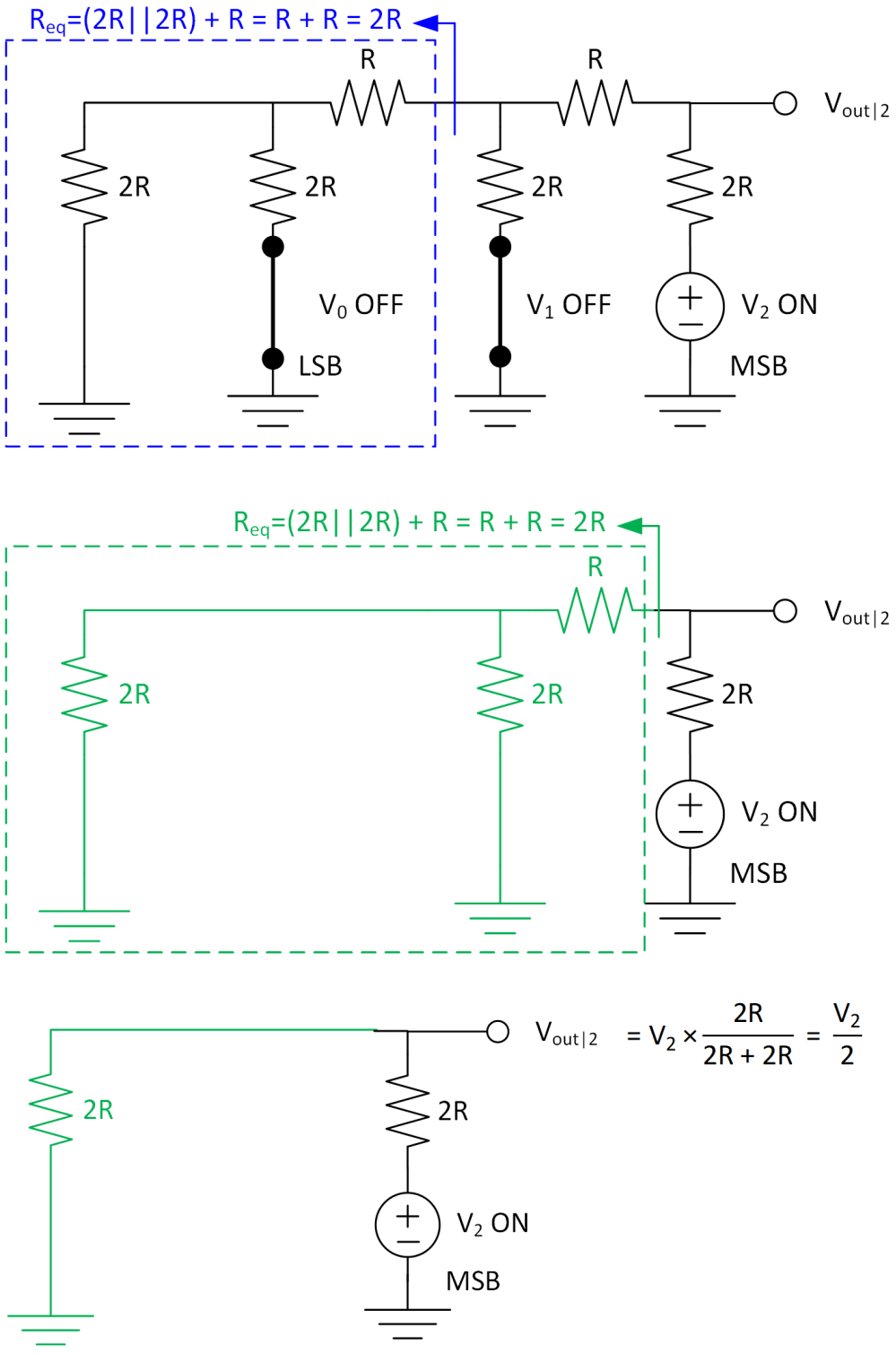
Now that we are done with the independent source V_0, we can repeat this for the other two independent sources. To find V_{out} due to independent source V_1 only, i.e. $V_{out|1}$:







Similarly, we can solve for $V_{out|2}$:



Putting it together, we have:

$$V_{\text{out}} = V_{\text{out}|0} + V_{\text{out}|1} + V_{\text{out}|2} = \frac{V_0}{8} + \frac{V_1}{4} + \frac{V_2}{2} \tag{12}$$

If we substitute for $V_0 = b_0 V_{\text{DD}}$, $V_1 = b_1 V_{\text{DD}}$, $V_2 = b_2 V_{\text{DD}}$, we get:

$$V_{\text{out}} = \frac{b_0 V_{\text{DD}}}{8} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_2 V_{\text{DD}}}{2} \tag{13}$$

which is the same result we found using KCL and Gaussian elimination in (9).

If you've made it this far, well done! Here's a challenge question for you. If instead of binary, imagine we are dealing with ternary numbers, i.e. $V_0 = t_0 V_{\text{DD}}$, $V_1 = t_1 V_{\text{DD}}$, $V_2 = t_2 V_{\text{DD}}$ where t_0, t_1, and t_2 can be -1, 0, or 1 ("ternary" means three possible values per digit). Assume we also want the output voltage levels to be evenly-spaced for all 27 ($= 3^3$) possible 3-digit ternary numbers. Can you design a resistor DAC to achieve this?

(b) **If $b_2, b_1, b_0 = 0, 1, 1$, what is V_{out}?** Express your answer in terms of V_{DD}.
Solution: Plugging into the equation (9) from part (a), we get

$$V_{\text{out}} = \frac{3V_{\text{DD}}}{8}. \tag{14}$$

(c) **If $b_2, b_1, b_0 = 1, 0, 1$, what is V_{out}?** Express your answer in terms of V_{DD}.
Solution: Plugging into the equation (9) from part (a), we get

$$V_{\text{out}} = \frac{5V_{\text{DD}}}{8}. \tag{15}$$

(d) **If $b_2, b_1, b_0 = 1, 1, 0$, what is V_{out}?** Express your answer in terms of V_{DD}.
Solution: Plugging into the equation (9) from part (a), we get

$$V_{\text{out}} = \frac{3V_{\text{DD}}}{4}. \tag{16}$$

(e) **If $b_2, b_1, b_0 = 1, 1, 1$, what is V_{out}?** Express your answer in terms of V_{DD}.
Solution: Plugging into the equation (9) from part (a), we get

$$V_{\text{out}} = \frac{7V_{\text{DD}}}{8}. \tag{17}$$

(f) **Explain how your results above show that the resistive DAC converts the 3-bit binary number (b_2, b_1, b_0) to the output analog voltage V_{out}.**
Solution: Every increment of $\frac{1}{8}V_{\text{DD}}$ on V_{DD} represents an increment of 1 to the 3-bit binary number $(b_2 b_1 b_0)$.
Alternatively, you can view V_{DD} as being 1 and then these are the first binary digits after the "decimal point."
For example, if $V_{\text{out}} = \frac{5}{8}V_{\text{DD}}$, the input was 5 in binary (1 0 1)$\rightarrow$ $(b_2 = 1\ b_1 = 0\ b_0 = 1)$.

4. Complex Numbers

Recall that a complex number $z \in \mathbb{C}$ is a number that can be expressed in the form

$$z = x + \mathrm{j}y \tag{18}$$

where $x, y \in \mathbb{R}$ and $j^2 = -1$. This is known as the Cartesian form of a complex number. We call x the real part of z and denote it $\mathrm{Re}\{z\} = x$. We call y the imaginary part of z and denote it $\mathrm{Im}\{z\} = y$.

Complex numbers can be visualized as vectors on the complex plane, as in Figure 1.

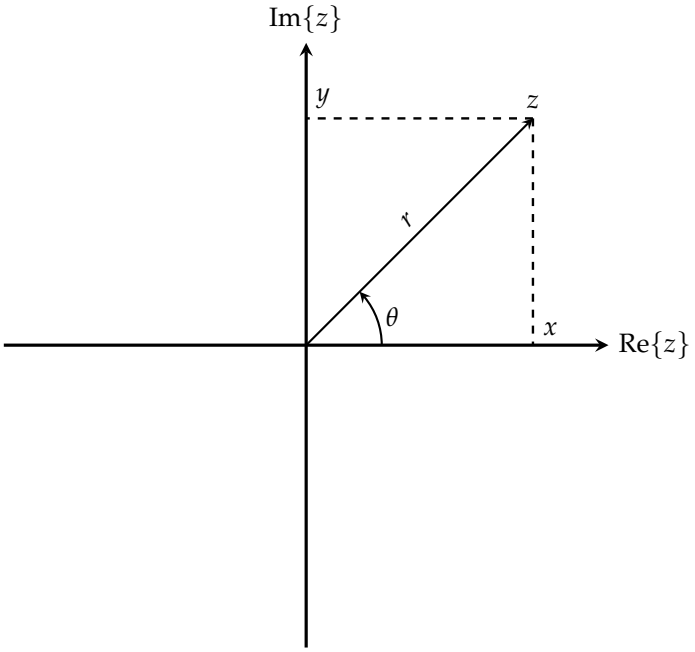


Figure 1: Complex plane

In this question, we will derive the polar form of a complex number and use this form to make some interesting conclusions.

(a) **Write an expression for the length of the vector z (as in Figure 1) in terms of x and y.** This is the magnitude of a complex number and is denoted by $|z|$ or r.
(*HINT: Use the Pythagorean theorem.*)
Solution:

$$r = \sqrt{x^2 + y^2} = |z| \tag{19}$$

(b) **Write expressions for x and y in terms of r and θ.**
Solution:

$$x = r\cos(\theta) \text{ and } y = r\sin(\theta) \tag{20}$$

(c) **Substitute for x and y in Equation 18.** Use Euler's identity[1] $\mathrm{e}^{\mathrm{j}\theta} = \cos(\theta) + \mathrm{j}\sin(\theta)$ to **conclude that**

$$z = r\mathrm{e}^{\mathrm{j}\theta}. \tag{21}$$

[1] also known as de Moivre's Theorem.

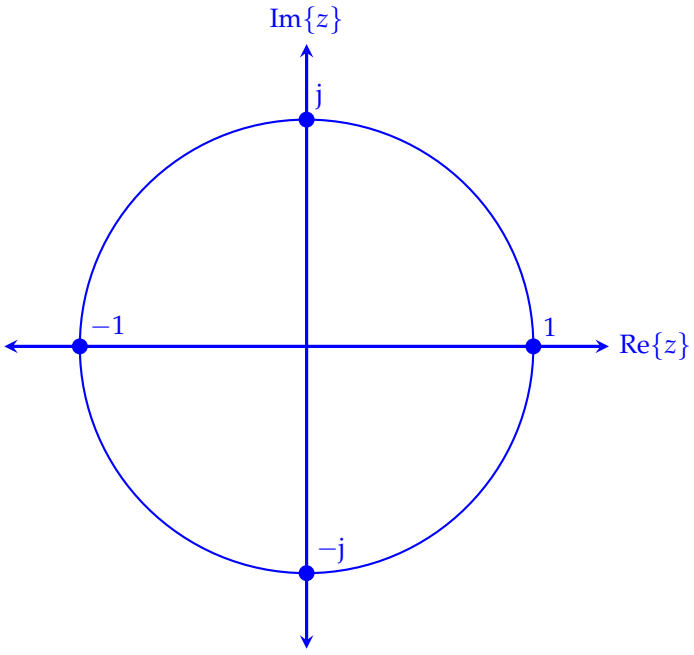
Solution:

$$z = r\cos(\theta) + \mathrm{j}r\sin(\theta) \tag{22}$$
$$= r(\cos(\theta) + \mathrm{j}\sin(\theta)) \tag{23}$$
$$= r\mathrm{e}^{\mathrm{j}\theta} \tag{24}$$

(d) In the complex plane, **sketch the set of all the complex numbers such that** $|z| = 1$. **What are the** z **values where the sketched figure intersects the real axis and the imaginary axis?**

Solution:

The set of all points on the complex plane the same distance from the origin is a circle. The circle we want is the unit circle, since the distance here is $|z| = 1$.



We have labeled the intersections with the real and imaginary axes above. Going counterclockwise: $1, \mathrm{j}, -1, -\mathrm{j}$. These happen to be the fourth roots of unity, a fact that will become important closer to the end of the course.

(e) Assume $z = r\mathrm{e}^{\mathrm{j}\theta}$. **Show that** $\overline{z} = r\mathrm{e}^{-\mathrm{j}\theta}$. Recall that the complex conjugate of a complex number $z = x + \mathrm{j}y$ is $\overline{z} = x - \mathrm{j}y$.

Solution:

$$\overline{z} = \overline{(r(\cos(\theta) + \mathrm{j}\sin(\theta)))} \tag{25}$$
$$= r(\cos(\theta) - \mathrm{j}\sin(\theta)) \tag{26}$$
$$= r(\cos(-\theta) + \mathrm{j}\sin(-\theta)) \tag{27}$$
$$= r\mathrm{e}^{-\mathrm{j}\theta} \tag{28}$$

Here, we used the facts that $\cos(-\theta) = \cos(\theta)$ and $\sin(-\theta) = -\sin(\theta)$ from trigonometry. You can also see these facts if you remember the Taylor series for cos and sin. Remember that the one for cos just has even powers of θ while the one for sin just has the odd ones.

(f) **Show (by direct calculation) that**

$$r^2 = z\overline{z}. \tag{29}$$

Solution:

$$z\bar{z} = re^{j\theta}re^{-j\theta} = r^2e^{j\theta-j\theta} = r^2e^0 = r^2. \tag{30}$$

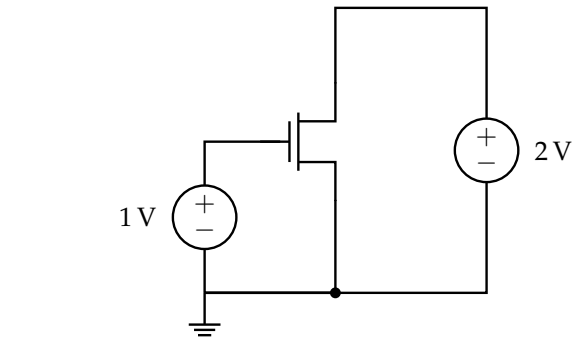
You can also do this in Cartesian coordinates:

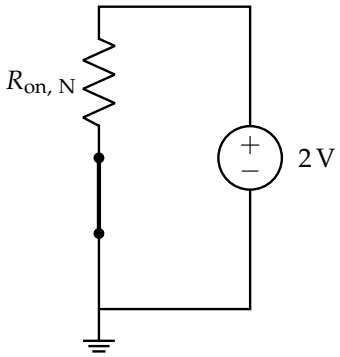
$$\begin{aligned} z\bar{z} &= r(\cos(\theta) + j\sin(\theta))r(\cos(\theta) - j\sin(\theta)) \\ &= r^2(\cos^2(\theta) - (j\sin(\theta))^2) \\ &= r^2(\cos^2(\theta) - j^2\sin^2(\theta)) \\ &= r^2(\cos^2(\theta) + \sin^2(\theta)) \\ &= r^2. \end{aligned}$$

5. Transistor Behavior

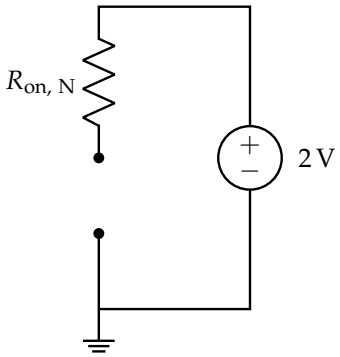
For all NMOS devices in this problem, $V_{tn} = 0.5\,\text{V}$. For all PMOS devices in this problem, $|V_{tp}| = 0.6\,\text{V}$.

(a) Which is the equivalent circuit as seen from the voltage source on the right-hand side of the circuit? **Fill in the correct bubble.**





Circuit A

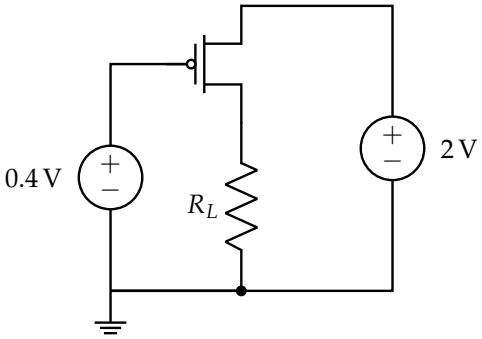


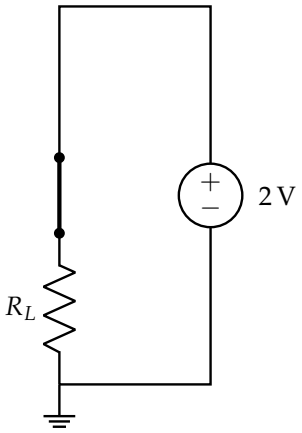
Circuit B

	A	B
Equivalent Circuit	◯	◯

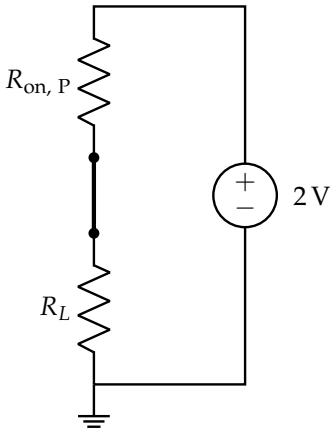
Solution: For the NMOS, $V_{GS} = 1\,\text{V} > V_{tn} = 0.5\,\text{V}$, so the NMOS transistor is on.
Thus circuit A is equivalent.

(b) Which is the equivalent circuit as seen form the voltage source on the right-hand side of the circuit? **Fill in the correct bubble.**

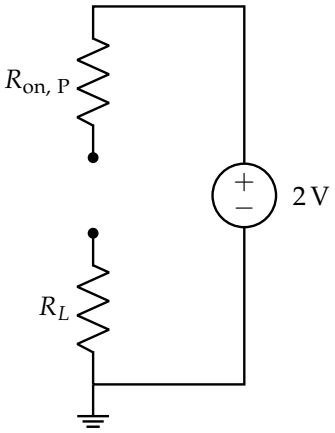




Circuit A



Circuit B

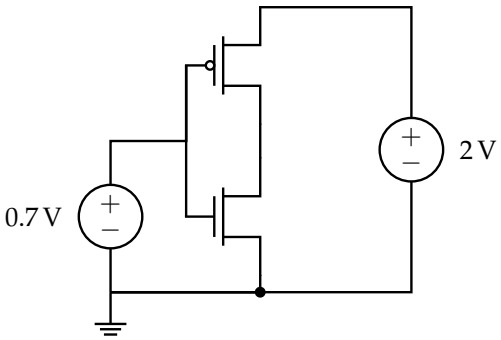


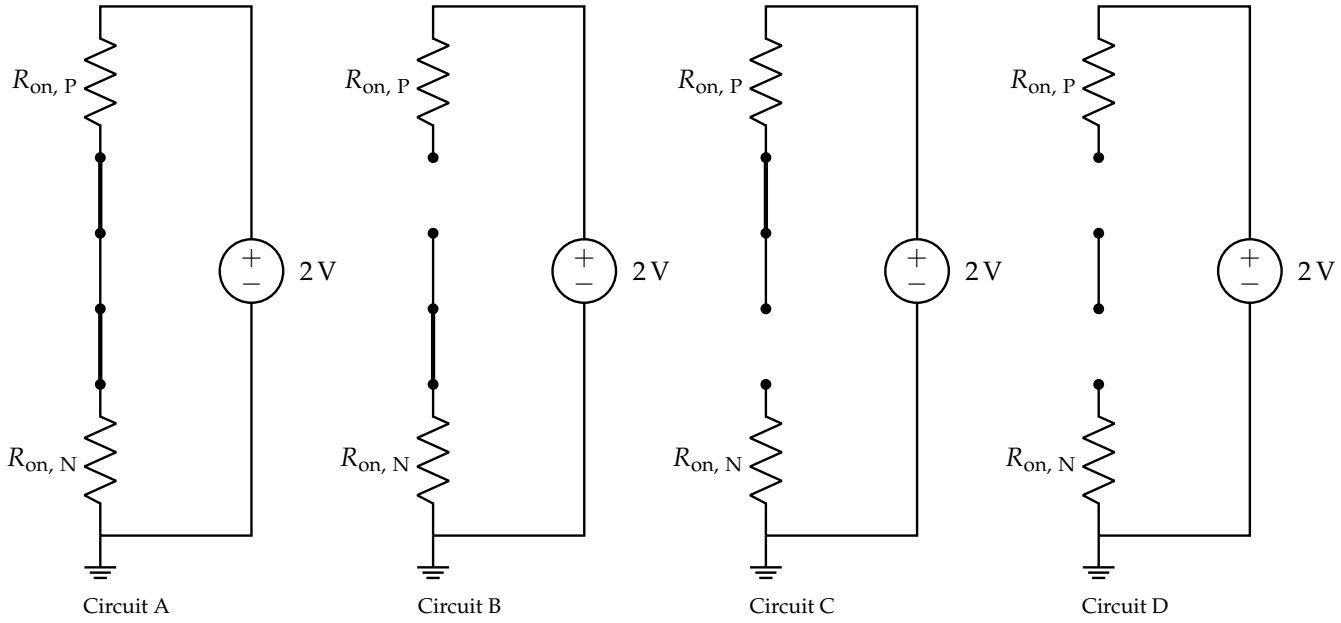
Circuit C

	A	B	C
Equivalent Circuit	◯	◯	◯

Solution: For the PMOS transistor, $|V_{GS}| = 1.6\,\text{V} > |V_{tp}| = 0.6\,\text{V}$, so the PMOS transistor is on. Thus circuit B is equivalent.

(c) Which is the equivalent circuit as seen form the voltage source on the right-hand side of the circuit? **Fill in the correct bubble.**





	A	B	C	D
Equivalent Circuit	◯	◯	◯	◯

Solution: For the PMOS transistor, $|V_{GS}| = 1.3\,\text{V} > |V_{tp}| = 0.6\,\text{V}$, so the PMOS transistor is on. For the NMOS transistor, $V_{GS} = 0.7\,\text{V} > V_{tn} = 0.5\,\text{V}$, so the NMOS transistor is on.

Note that in this case, both transistors are on.

Thus circuit A is equivalent.

Aside: In digital logic, it is usually undesirable to have this state in your system for several reasons. First, the output voltage of the inverter (the voltage at the shared drain of the NMOS and PMOS) will not be either 0 or V_{DD}, which means the output voltage is not at 'true' binary value. In addition, we now have a direct current path through the NMOS and PMOS transistors from VDD to ground. This will burn a lot of power! In reality, all inverters briefly transition through this state where both NMOS and PMOS are on when the inputs change from 1 to 0 or 0 to 1.

6. Existence and uniqueness of solutions to differential equations

When doing circuits or systems analysis, we sometimes model our system via a differential equation, and would often like to solve it to get the system trajectory. To this end, we would like to verify that a solution to our differential equation exists and is unique, so that our model is physically meaningful. There is a general approach to doing this, which is demonstrated in this problem.

We would like to show that there is a unique function $x\colon \mathbb{R} \to \mathbb{R}$ which satisfies

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \alpha x(t) \tag{31}$$

$$x(0) = x_0. \tag{32}$$

In order to do this, we will first verify that a solution x_d exists. To show that x_d is the unique solution, we will take an arbitrary solution y and show that $x_d(t) = y(t)$ for every t.

(a) First, let us show that a solution to our differential equation exists. **Verify that $x_d(t) := x_0 e^{\alpha t}$ satisfies eq. (31) and eq. (32).**

Solution: We first verify eq. (31).

$$\frac{\mathrm{d}}{\mathrm{d}t}x_d(t) = \frac{\mathrm{d}}{\mathrm{d}t}\left(x_0 e^{\alpha t}\right) \tag{33}$$

$$= x_0 \frac{\mathrm{d}}{\mathrm{d}t} e^{\alpha t} \tag{34}$$

$$= x_0 \cdot \alpha e^{\alpha t} \tag{35}$$

$$= \alpha \cdot x_0 e^{\alpha t} \tag{36}$$

$$= \alpha x_d(t). \tag{37}$$

Now we verify eq. (32).

$$x_d(0) = x_0 e^{\alpha \cdot 0} \tag{38}$$

$$= x_0 e^0 \tag{39}$$

$$= x_0. \tag{40}$$

(b) Now, let us show that our solution is unique. As mentioned before, suppose $y\colon \mathbb{R} \to \mathbb{R}$ also satisfies eq. (31) and eq. (32).

We want to show that $y(t) = x_d(t)$ for all t. Our strategy is to show that $\frac{y(t)}{x_d(t)} = 1$ for all t.

However, this particular differential equation poses a problem: if $x_0 = 0$, then $x_d(t) = 0$ for all t, so that the quotient is not well-defined. To patch this method, we would like to avoid using any function with x_0 in the denominator. One way we can do this is consider a modification of the quotient $\frac{y(t)}{x_d(t)} = \frac{y(t)}{x_0 e^{\alpha t}}$; in particular, we consider the function $z(t) := \frac{y(t)}{e^{\alpha t}}$.

Show that $z(t) = x_0$ for all t, and explain why this means that $y(t) = x_d(t)$ for all t.

(*HINT: Show first that $z(0) = x_0$ and then that $\frac{\mathrm{d}}{\mathrm{d}t}z(t) = 0$. Argue that these two facts imply that $z(t) = x_0$ for all t. Then show that this implies $y(t) = x_d(t)$ for all t.*)

(*HINT: Remember that we said y is any solution to eq. (31) and eq. (32), so we only know these properties of y. If you need something about y to be true, see if you can show it from eq. (31) and eq. (32).*)

(*HINT: When taking $\frac{\mathrm{d}}{\mathrm{d}t}z(t)$, remember to use the quotient rule, along with what we know about y.*)

Solution: The solution goes in four stages, as per the hint.

Step 1. We show that $z(0) = x_0$. Indeed, using eq. (32),

$$z(0) = \frac{y(0)}{e^{\alpha \cdot 0}} = \frac{x_0}{e^0} = \frac{x_0}{1} = x_0. \tag{41}$$

Step 2. We show that $\frac{\mathrm{d}}{\mathrm{d}t}z(t) = 0$. Indeed, using the quotient rule from calculus and eq. (31),

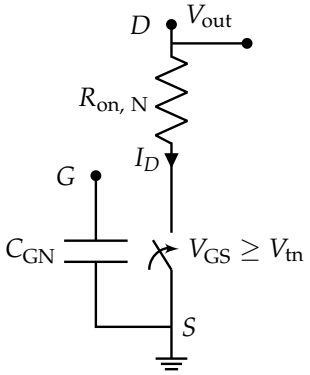
$$\begin{aligned}
\frac{\mathrm{d}}{\mathrm{d}t}z(t) &= \frac{\mathrm{d}}{\mathrm{d}t}\frac{y(t)}{\mathrm{e}^{\alpha t}} && (42)\\
&= \frac{\mathrm{e}^{\alpha t}\left(\frac{\mathrm{d}}{\mathrm{d}t}y(t)\right) - y(t)\left(\frac{\mathrm{d}}{\mathrm{d}t}\mathrm{e}^{\alpha t}\right)}{\mathrm{e}^{2\alpha t}} && (43)\\
&= \frac{\mathrm{e}^{\alpha t}(\alpha y(t)) - y(t)\left(\alpha \mathrm{e}^{\alpha t}\right)}{\mathrm{e}^{2\alpha t}} && (44)\\
&= \frac{\alpha \mathrm{e}^{\alpha t} y(t) - \alpha \mathrm{e}^{\alpha t} y(t)}{\mathrm{e}^{2\alpha t}} && (45)\\
&= \frac{0}{\mathrm{e}^{2\alpha t}} && (46)\\
&= 0. && (47)
\end{aligned}$$

Step 3. We show that $z(t) = x_0$ for all t. Indeed, since $\frac{\mathrm{d}}{\mathrm{d}t}z(t) = 0$, we know that $z(t)$ is a constant. Since $z(0) = x_0$, this gives that $z(t)$ is the constant value x_0, and hence $z(t) = x_0$ for all t.

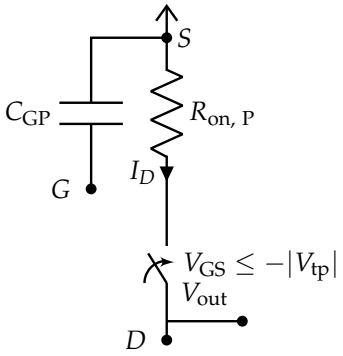
Step 4. We show that $y(t) = x_d(t)$ for all t. Indeed, since $z(t) = x_0$ and $z(t) = \frac{y(t)}{\mathrm{e}^{\alpha t}}$, we have $x_0 = \frac{y(t)}{\mathrm{e}^{\alpha t}}$. We multiply both sides by $\mathrm{e}^{\alpha t}$ to get $y(t) = x_0\mathrm{e}^{\alpha t}$. But this is just $x_d(t)$, so $y(t) = x_d(t)$ for all t.

7. Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model



(b) PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on,\,N} = R_{on,\,P} = 1\,\text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1$ fF (fF = femto-Farads = 1×10^{-15} F). We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 9).

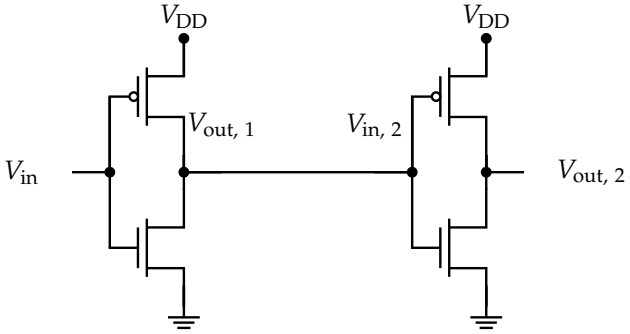


Figure 9: CMOS Inverter chain

(a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$).

Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,\,1}$) for time $t \geq 0$.

Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

Solution: To analyze this circuit as an RC circuit we can recall the transistor switch model. Using this we can see that the first inverter's output appears as a resistor connected to V_{DD} when the input is low (NMOS off, PMOS on), or a resistor connected to ground when the input turns high (NMOS on, PMOS off).

Before $t = 0$, the input to the first inverter was low for a long time. This means that for $t < 0$, the output of the inverter ($V_{out,\,1}$) had been held at V_{DD} for a long time.

At $t = 0$, the input goes high, which means that the input inverter's NMOS device turns on, connecting $V_{\text{out, 1}}$ to ground through a resistance of R_{on}.

The second inverter "loads" the output of the first inverter. From the notes in the problem, we can model the gates of the transistors as capacitors. These gates together form our capacitive load. The gate of the PMOS acts as a capacitor to V_{DD} and the gate of the NMOS acts as a capacitor to ground.

Using this we can draw the following RC circuit:

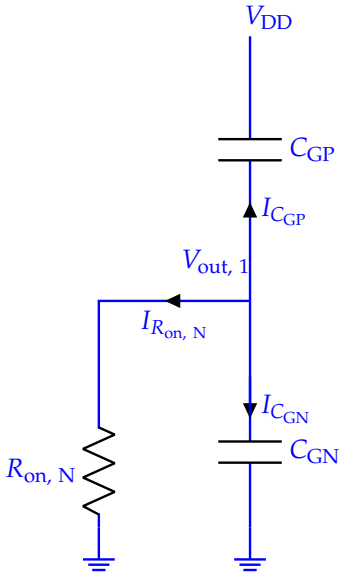


Figure 10: First inverter output at 0

To get the differential equation describing the output of the first inverter at time $t \geq 0$ let us first think about the behavior of the circuit at and after $t = 0$.

Before $t = 0$ we know that the output $V_{\text{out, 1}} = V_{\text{DD}}$. This means that C_{GN} is charged, while C_{GP} is not as there is no voltage difference across it.

At $t = 0$, when the input to the first inverter changes (input switches to high), the NMOS will turn on, discharging the $V_{\text{out, 1}}$ node. Thus $V_{\text{out, 1}}$ will eventually discharge to zero in steady state.

We know the voltage across C_{GP} is $V_{\text{out, 1}}(t) - V_{\text{DD}}$ and the voltage across C_{GN} is $V_{\text{out, 1}}(t)$. Using this information we can set up a differential equation to solve for $V_{\text{out}}(t)$.

Writing the expressions for the three branch currents yields:

$$I_{C_{\text{GP}}} = C_{\text{GP}} \frac{\mathrm{d}}{\mathrm{d}t}(V_{\text{out, 1}}(t) - V_{\text{DD}}) \tag{48}$$

$$I_{C_{\text{GN}}} = C_{\text{GN}} \frac{\mathrm{d}}{\mathrm{d}t} V_{\text{out, 1}}(t) \tag{49}$$

$$I_{R_{\text{on, N}}} = \frac{V_{\text{out, 1}}(t)}{R_{\text{on, N}}} \tag{50}$$

Writing KCL at the single node yields:

$$I_{C_{\text{GP}}} + I_{C_{\text{GN}}} + I_{R_{\text{on, N}}} = 0 \tag{51}$$

in other words:

$$I_{C_{\text{GP}}} + I_{C_{\text{GN}}} = -I_{R_{\text{on, N}}} \tag{52}$$

Expanding the branch currents with their expressions:

$$C_{GP}\frac{d}{dt}(V_{out,1}(t)-V_{DD})+C_{GN}\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}(t)}{R_{on,N}} \tag{53}$$

$$C_{GP}\frac{d}{dt}V_{out,1}(t)+C_{GN}\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}(t)}{R_{on,N}} \tag{54}$$

$$(C_{GP}+C_{GN})\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}(t)}{R_{on,N}} \tag{55}$$

Re-writing as a first-order differential equation for $V_{out,1}$ yields:

$$\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}(t)}{R_{on,N}(C_{GP}+C_{GN})} \tag{56}$$

(b) Given the initial conditions in part (a), **solve for** $V_{out,1}(t)$**.**

Solution: We know that the solution to a differential equation of the form

$$\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}}{R_{on,N}(C_{GP}+C_{GN})} \tag{57}$$

is

$$V_{out,1}(t)=ke^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}} \tag{58}$$

Plugging in the initial condition $V_{out,1}(0)=V_{DD}$ we find that $V_{out,1}(t)=V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}$.

(c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

Solution:

(1) We know that the output of our inverter started with the initial value V_{DD}.

(2) Since the differential equation tells us the change in value of $V_{out,1}(t)$ at time t we can simply plug in $t=0$ into our differential equation to get the initial slope:

$$\frac{d}{dt}V_{out,1}(t)=-\frac{V_{out,1}(0)}{R_{on,N}(C_{GP}+C_{GN})} \tag{59}$$

$$\frac{d}{dt}V_{out,1}(t)=-\frac{V_{DD}}{R_{on,N}(C_{GP}+C_{GN})} \tag{60}$$

Thus the initial slope is $-\frac{V_{DD}}{R_{on,N}(C_{GP}+C_{GN})}$.

(3) Since the input to the inverter changed from low to high we know the output of the first inverter ($V_{out,1}$) is going to go to 0 in steady state, as this node will be discharged by the first inverter's NMOS transistor.
Alternatively, we can find the asymptotic value by plugging in $t=\infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1}=V_{DD}e^{-\frac{\infty}{R_{on,N}(C_{GP}+C_{GN})}}=0$.

(4) To approximate when the output will decay to $\frac{1}{3}$ its original value, we use the fact that $e^{-1}=\frac{1}{e}\approx\frac{1}{3}$. We thus want to find when $V_{out,1}=V_{DD}e^{-1}$.
This will occur when the e term is raised to -1, which occurs when $t=R_{on,N}(C_{GP}+C_{GN})=2\times10^{-12}$s.
You should also give yourself full credit if you used $\frac{1}{3}$ itself and computed $-\ln(3)$, etc.

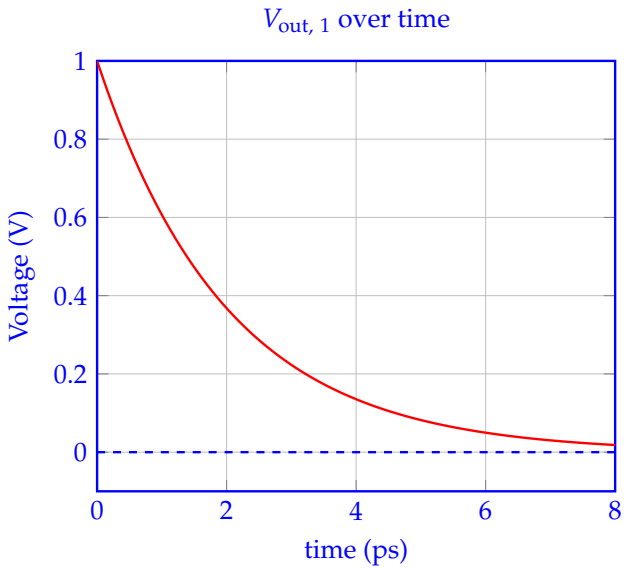


Figure 11

(d) A long time later, the input to the first inverter switches low again.
Solve for $V_{\text{out, 1}}(t)$.
Sketch the output voltage of the first inverter ($V_{\text{out, 1}}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.
Solution: We know that after a long time, the output of the first inverter has stabilized to 0. When the input switches low again, the input inverter's NMOS device turns off, while the input inverter's PMOS device turns on. This connects the $V_{\text{out, 1}}$ node to V_{DD}, as shown in Figure 12.

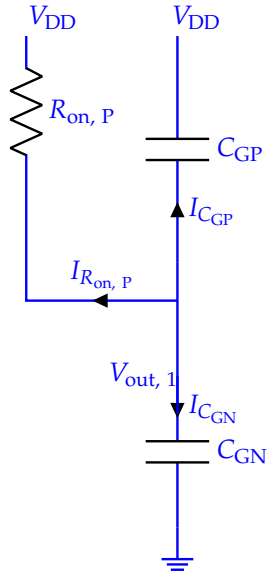


Figure 12: Inverter output at 1

To set up the differential equation, we apply KVL and KCL again:

$$I_{C_{\text{GP}}} = C_{\text{GP}} \frac{\text{d}}{\text{d}t}(V_{\text{out, 1}}(t) - V_{\text{DD}}) \tag{61}$$

$$I_{C_{GN}} = C_{GN}\frac{d}{dt}V_{out,\,1}(t) \tag{62}$$

$$I_{R_{on,\,P}} = \frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{63}$$

$$I_{C_{GP}} + I_{C_{GN}} = -I_{R_{on,\,P}} \tag{64}$$

$$C_{GP}\frac{d}{dt}(V_{out,\,1}(t) - V_{DD}) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{65}$$

$$C_{GP}\frac{d}{dt}V_{out,\,1}(t) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{66}$$

$$(C_{GP} + C_{GN})\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{67}$$

$$\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}(C_{GP} + C_{GN})} \tag{68}$$

We will use substitution of variables:

$$x(t) = V_{out,\,1}(t) - V_{DD} \tag{69}$$

$$V_{out,\,1}(t) = x(t) + V_{DD} \tag{70}$$

$$\frac{d}{dt}x(t) = \frac{d}{dt}V_{out,\,1}(t) \tag{71}$$

Substituting in:

$$\frac{d}{dt}x(t) = -\frac{x}{R_{on,\,P}(C_{GP} + C_{GN})} \tag{72}$$

$$x(t) = Ae^{-\frac{t}{R_{on,\,P}(C_{GP}+C_{GN})}} \tag{73}$$

Substituting again for $x(t)$:

$$V_{out,\,1}(t) = V_{DD} + Ae^{-\frac{t}{R_{on,\,P}(C_{GP}+C_{GN})}} \tag{74}$$

Using the initial condition $V_{out,\,1} = 0$ (as the input to the first inverter was high for a long time before switching low) implies $A = -V_{DD}$. Thus:

$$V_{out,\,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_{on,\,P}(C_{GP}+C_{GN})}}\right) \tag{75}$$

(1) Because the input to the first inverter was high for a long time, we know the initial value of $V_{out,\,1}(t) = 0$. This was the initial condition applied to the solution of the differential equation, above.

(2) To find the initial value of the slope we can plug in $t = 0$ to the above differential equation:

$$\frac{d}{dt}V_{out,\,1}(t) = \frac{(V_{DD} - V_{out,\,1}(0))}{R_{on,\,P}(C_{GP} + C_{GN})} \tag{76}$$

where $V_{out,\,1}(0) = 0$. Thus our initial slope is $\frac{(V_{DD})}{R_{on,\,P}(C_{GP}+C_{GN})}$. Notice this slope is positive while the previous part had a negative slope.

(3) Since the input to the inverter changed from low to high and the input inverter's PMOS is now on, we know the output of the first inverter is going to go to V_{DD} in steady state.

(4) Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,\,1}(t)$ to find $V_{out,\,1} = V_{DD}\left(1 - e^{-\frac{\infty}{R_{on,\,P}(C_{GP}+C_{GN})}}\right) = V_{DD}(1 - 0) = V_{DD}$.

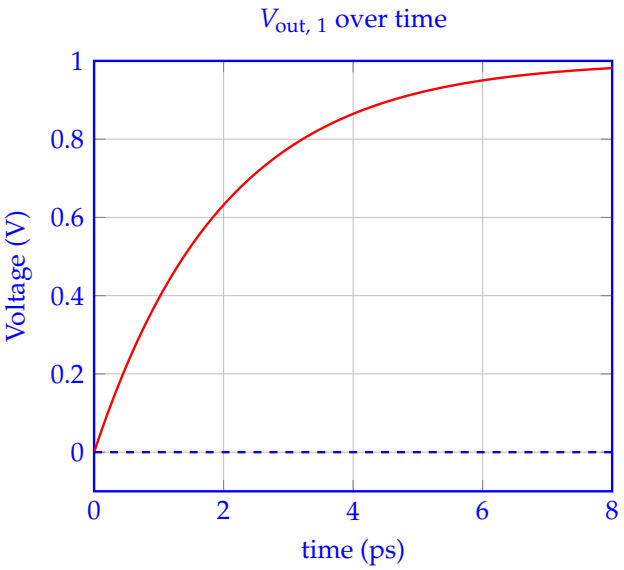


Figure 13

8. **(OPTIONAL) Make Your Own Problem.**

   Write your own problem about content covered in the course thus far, and provide a thorough solution to it.

   NOTE: This can be a totally new problem, a modification on an existing problem, or a Jupyter part for a problem that previously didn't have one. Please cite all sources for anything (including course material) that you used as inspiration.

   NOTE: High-quality problems may be used as inspiration for the problems we choose to put on future homeworks or exams.

9. **Homework Process and Study Group**

   Citing sources and collaborators are an important part of life, including being a student!

   We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

   (a) **What sources (if any) did you use as you worked through the homework?**

   (b) **If you worked with someone on this homework, who did you work with?**
   List names and student ID's. (In case of homework party, you can also just describe the group.)

   (c) **Roughly how many total hours did you work on this homework? Write it down here where you'll need to remember it for the self-grade form.**

Contributors:

- Edward Wang.
- Ayan Biswas.
- Wahid Rahman.
- Siddharth Iyer.
- Sidney Buchbinder.
- Anant Sahai.
- Nikhil Shinde.
- Druv Pai.
- Kris Pister.
- Regina Eckert.
- Gaoyue Zhou.