Review Worksheet 1

1. Logic Gates

In digital design, we often use 'synchronous' circuits, i.e. circuits which evaluate when a clock signal transitions from 0 to V_{DD}. One such implementation, called domino CMOS logic, is shown in Figure 1. Initially $V_{\text{clk}} = 0$ ('reset phase') for a long time, so the output node is high, i.e. $V_{\text{out}} = V_{DD}$ and the capacitor is fully charged, regardless of the values of V_A and V_B. We want to complete the Truth Table 1 during the 'evaluation phase'.

For cases (ii) and (iv), when V_{clk} transitions from 0 to V_{DD} and V_A and V_B are equal to the values specified in the table, what is V_{out}? Justify your answer.

Note that if all transistors connected to the output node are switched off, then the capacitor C at the output node 'holds' the voltage since there is no charging / discharging path in that case.

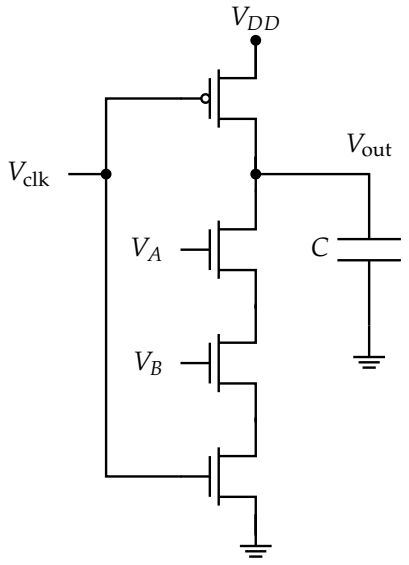


Figure 1: Domino Logic Gate

Solution:

Case	V_{clk}	V_A	V_B	V_{out}
(i)	$0 \to V_{DD}$	0	0	$V_{DD} \to V_{DD}$
(ii)	$0 \to V_{DD}$	0	V_{DD}	$V_{DD} \to$?
(iii)	$0 \to V_{DD}$	V_{DD}	0	$V_{DD} \to V_{DD}$
(iv)	$0 \to V_{DD}$	V_{DD}	V_{DD}	$V_{DD} \to$?

Table 1: Truth Table

Solution: Since $V_{\text{clk}} = V_{DD}$, the PMOS is switched off and the NMOS closest to ground is switched on.
In Case (ii), $V_A = 0$, which means the corresponding NMOS is switched off, so the entire NMOS network is 'off'. Hence the output node is floating, so it stays at the voltage stored in the capacitor, hence $V_{\text{out}} = V_{DD}$.
In Case (iv), is $V_A = V_{DD}$ and $V_B = V_{DD}$, so all the NMOS are switched on and the output node can discharge to ground. Hence $V_{\text{out}} = 0$. The complete truth table is shown in Table 2.

Case	V_{clk}	V_A	V_B	V_{out}
(i)	$0 \to V_{DD}$	0	0	$V_{DD} \to V_{DD}$
(ii)	$0 \to V_{DD}$	0	V_{DD}	$V_{DD} \to V_{DD}$
(iii)	$0 \to V_{DD}$	V_{DD}	0	$V_{DD} \to V_{DD}$
(iv)	$0 \to V_{DD}$	V_{DD}	V_{DD}	$V_{DD} \to 0$

Table 2: Truth Table

From the truth table, we can see that this is a NAND gate.

2. Analog Signal Processing

In this problem, we will study an example of one of the most common applications in signal processing: removing noise and amplifying the desired signal in a receiver.

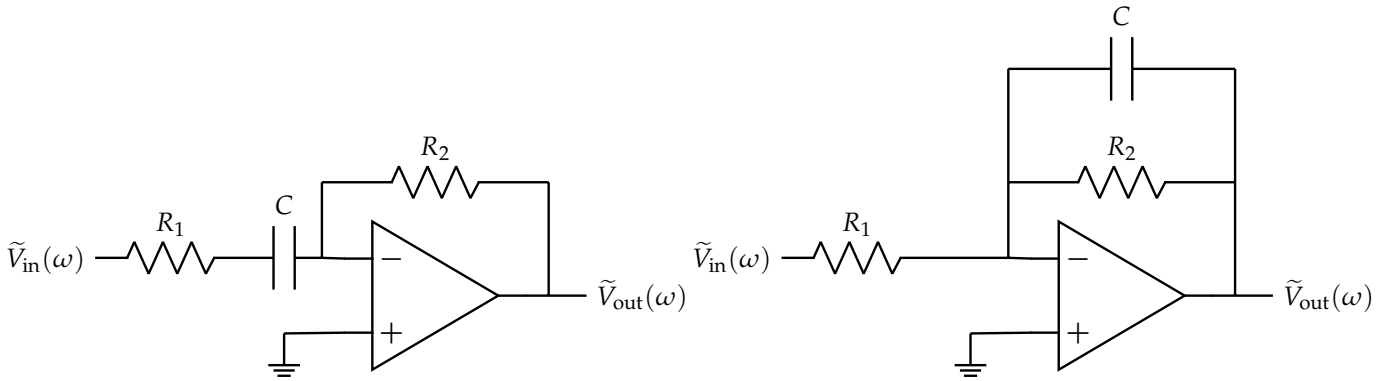
In 16B we have learned about filters, so we can selectively remove specific noise frequency bands. Assume that we have a low frequency desired signal $s(t) = \cos(\omega_{\text{sig}} t)$, where $\omega_{\text{sig}} = 10\frac{\text{rad}}{\text{s}}$, and a high frequency noise $n(t) = 2\cos(\omega_{\text{noise}} t)$, where $\omega_{\text{noise}} = 1000\frac{\text{rad}}{\text{s}}$, at the receiver input. We wish to amplify the desired signal and also reject the noise.

(a) Let's first attempt to use a low-pass filter to achieve this goal. Since we wish to amplify the desired signal, we need to use a low-pass filter with gain > 1 (i.e. use an amplifier combined with a filter). Assume that the op-amps are ideal and follow the golden rules.

i. **Derive a transfer function for the filter configuration in Figure 2a.** Show your work.

ii. **Derive a transfer function for the filter configuration in Figure 2b.** Show your work.

iii. Out of the two filter configurations in Figure 2, **which one is the low-pass filter? Justify your answer.**



(a) Config 1 **(b)** Config 2

Figure 2: Active filter receiver configurations

Solution:

i. For the first configuration in Figure 2a,

$$Z_{\text{in},1} = R_1 + \frac{1}{j\omega C} \tag{1}$$

$$Z_{\text{fb},1} = R_2 \tag{2}$$

$$H_1(\omega) = \frac{\widetilde{V}_{\text{out}}(\omega)}{\widetilde{V}_{\text{in}}(\omega)} = -\frac{Z_{\text{fb},1}}{Z_{\text{in},1}} \tag{3}$$

$$= -\frac{R_2}{R_1 + \frac{1}{j\omega C}} \tag{4}$$

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$$= -\frac{j\omega CR_2}{1+j\omega CR_1} = -\frac{R_2}{R_1}\cdot\frac{1}{1-\frac{j}{\omega CR_1}} \tag{5}$$

Notice, that this transfer function has a gain component $\left(-\frac{R_2}{R_1}\right)$ and a high-pass filter component $\left(\frac{1}{1-\frac{j}{\omega CR_1}}\right)$.

ii. For the second configuration in Figure 2b,

$$Z_{\text{in},2} = R_1 \tag{6}$$

$$Z_{\text{fb},2} = R_2 \parallel \frac{1}{j\omega C} = \frac{R_2}{1+j\omega CR_2} \tag{7}$$

$$H_2(\omega) = \frac{\widetilde{V}_{\text{out}}(\omega)}{\widetilde{V}_{\text{in}}(\omega)} = -\frac{Z_{\text{fb},2}}{Z_{\text{in},2}} \tag{8}$$

$$= -\frac{R_2}{R_1}\cdot\frac{1}{1+j\omega CR_2} \tag{9}$$

Notice, that this transfer function has a gain component $\left(-\frac{R_2}{R_1}\right)$ and a low-pass filter component $\left(\frac{1}{1+j\omega CR_2}\right)$.

iii. Analyzing the transfer functions of the two configurations we see that Config 2 represents a low-pass filter. Example justification answers - Config 2 transfer function has a single pole. Looking at frequency extremes $\omega \to 0$ and $\omega \to \infty$ we conclude that the Config 2 transfer function represents a low-pass filter.

(b) Suppose that the transfer function of the low-pass filter with gain from part (a) was $H_{\text{LPF}}(\omega) = -\frac{A}{1+j\frac{\omega}{\omega_c}}$, where the cutoff frequency frequency is $\omega_c = 100\frac{\text{rad}}{\text{s}}$ and the gain is $A = 10$. The Bode plots for the low-pass filter with gain are shown below. Read-off the numerical values corresponding to the appropriate points on the Bode plots.

i. What are the magnitude and phase of the filter output signal when the input into the filter is $s(t) = \cos(\omega_{\text{sig}}t)$, where $\omega_{\text{sig}} = 10\frac{\text{rad}}{\text{s}}$? **Derive the time domain expression for the filter output signal.**

ii. What are the magnitude and phase of the filter output signal when the input into the filter is $n(t) = 2\cos(\omega_{\text{noise}}t)$, where $\omega_{\text{noise}} = 1000\frac{\text{rad}}{\text{s}}$? **Derive the time domain expression for the filter output signal.**

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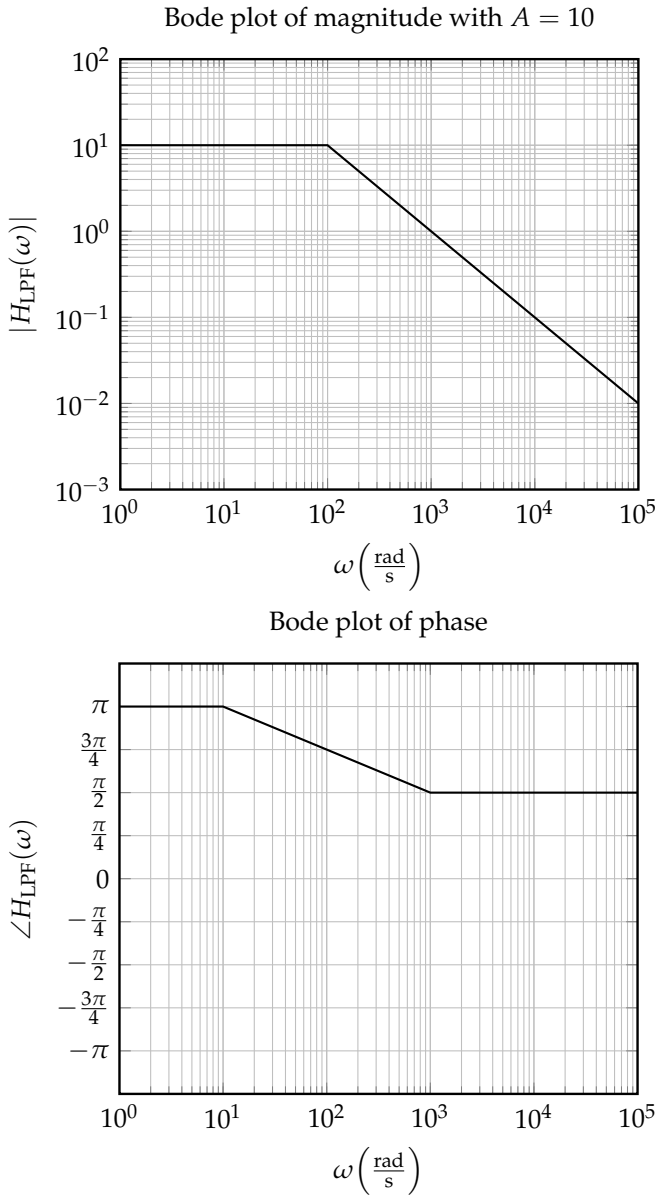

Solution:

i. From the Bode plots, we can read that $H_{\text{LPF}}(\omega_{\text{sig}}) = 10e^{j\pi}$. Hence

$$s(t) = \cos(10t) \tag{10}$$
$$\implies \widetilde{S} = 0.5e^{j0} \tag{11}$$
$$\implies \widetilde{S_1} = \widetilde{S} \cdot H_{\text{LPF}}(\omega_{\text{sig}}) \tag{12}$$
$$= 5e^{j\pi} \tag{13}$$
$$\implies s_1(t) = 10\cos(10t + \pi) = -10\cos(10t) \tag{14}$$

Alternatively, realize that the transfer function directly affects the signal amplitude and phase to write the time domain answer $s_1(t) = 10\cos(10t + \pi) = -10\cos(10t)$.

ii. From the Bode plots, we can read that $H_{\text{LPF}}(\omega_{\text{noise}}) = e^{j\frac{\pi}{2}}$. Hence

$$n(t) = 2\cos(1000t) \tag{15}$$

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$$\implies \widetilde{N} = e^{j0} \tag{16}$$

$$\implies \widetilde{N_1} = \widetilde{N} \cdot H_{\text{LPF}}(\omega_{\text{noise}}) \tag{17}$$

$$= e^{j\frac{\pi}{2}} \tag{18}$$

$$\implies n_1(t) = 2\cos\left(1000t + \frac{\pi}{2}\right) = -2\sin(1000t) \tag{19}$$

Alternatively, realize that the transfer function directly affects the noise amplitude and phase to write the time domain answer $n_1(t) = 2\cos\left(1000t + \frac{\pi}{2}\right) = -2\sin(1000t)$.

(c) We wish to have the signal be more amplified with respect to the noise. One approach is to cascade two copies of the filter $H_{\text{LPF}}(\omega)$ to make a second-order low-pass filter with gain. Note that it is not necessary to put a unity gain buffer between the two filters, because the V_{out} loading **does not affect** the behavior of this specific filter configuration.

i. **Derive the transfer function $H_{\text{casc}}(\omega)$ of the second-order low-pass filter** by cascading 2 of the first order transfer function $H_{\text{LPF}}(\omega) = -\frac{A}{1+j\frac{\omega}{\omega_c}}$ from part (b) with $\omega_c = 100\frac{\text{rad}}{\text{s}}$ and $A = 10$. **Show your work.**

ii. **Sketch the Bode magnitude and phase plots of $H_{\text{casc}}(\omega)$ on the charts in your answer template.**

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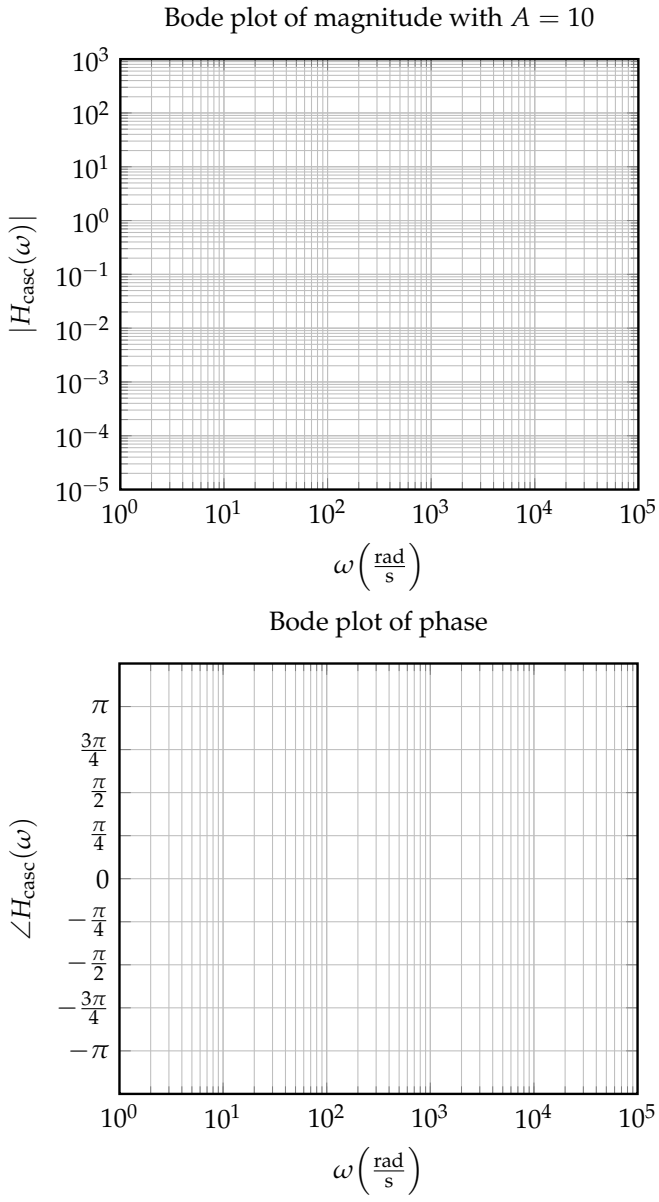

(HINT: Pay attention to the direction of the slopes.)

Solution:

i. Since there is no loading effect, the transfer function of the cascaded filter is

$$H_{\text{casc}}(\omega) = H_{\text{LPF}}^2(\omega) \tag{20}$$

$$= \frac{A^2}{(1 + \text{j}\frac{\omega}{\omega_c})^2} \tag{21}$$

ii. The Bode magnitude plot satisfies the following properties:

- At frequencies $\omega \leq \omega_c = 100\frac{\text{rad}}{\text{s}}$, magnitude is $A^2 = 100$.
- At frequencies $\omega > \omega_c = 100\frac{\text{rad}}{\text{s}}$, magnitude drops by $100\times$ per power of 10 of ω.

The Bode phase plot satisfies the following properties:

- At frequencies $\omega \leq \frac{\omega_c}{10} = 10\frac{\text{rad}}{\text{s}}$, phase is $0\,\text{rad} = 0°$.

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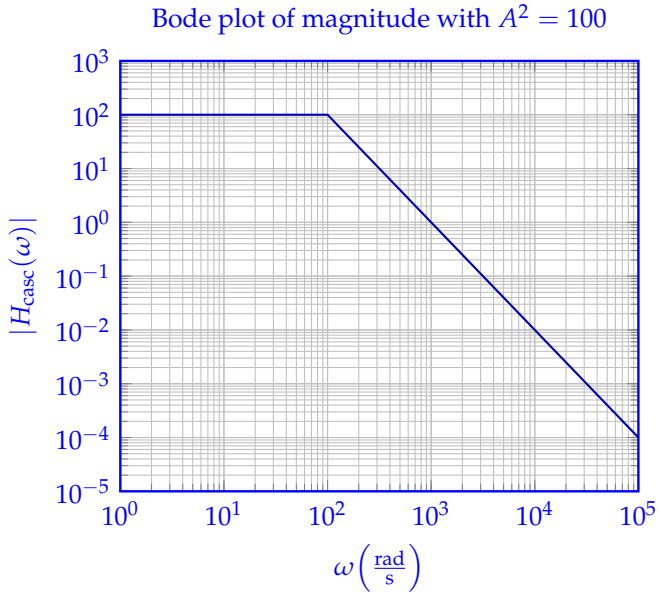
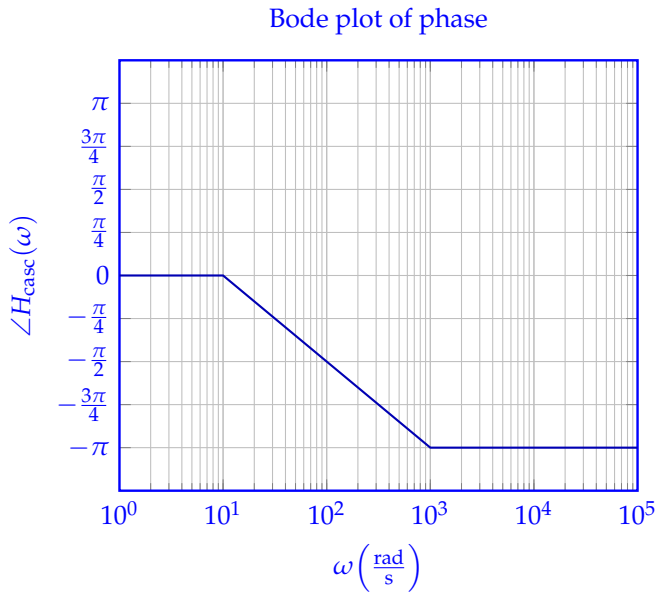
- At frequencies $\omega \geq 10\omega_c = 1000\frac{\text{rad}}{\text{s}}$, phase is $-\pi$ rad $= -180°$.
- At $\omega = \omega_c = 100\frac{\text{rad}}{\text{s}}$, phase is $-\frac{\pi}{2}$ rad $= -90°$.





(d) Our implementation of the cascaded second-order filter from part (c) uses 2 op-amps. Can we get even more noise attenuation by using a single op-amp? One approach is to use a Notch filter that ideally completely rejects the noise.

Let's consider the cascade of an LC Notch filter with a non-inverting amplifier in Figure 3. We wish to have a notch at the noise frequency so that the noise $n(t) = 2\cos(\omega_{\text{noise}}t)$, where $\omega_{\text{noise}} = 1000\frac{\text{rad}}{\text{s}}$, is completely rejected, while the the signal $s(t) = \cos(\omega_{\text{sig}}t)$, where $\omega_{\text{sig}} = 10\frac{\text{rad}}{\text{s}}$, is amplified.

i. **Derive the transfer function $H_{\text{notch}}(\omega) = \frac{\tilde{V}_{\text{out}}(\omega)}{\tilde{V}_{\text{in}}(\omega)}$ of the filter in Figure 3.** Assume that the op-amp is ideal and follows the golden rules. Show your work.

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ii. Using $C = 0.5\,\text{mF}$, **find the inductance value L so that the notch (i.e. the frequency at which the magnitude of the transfer function is 0) is at the noise frequency $\omega_{\text{noise}} = 1000\frac{\text{rad}}{\text{s}}$.** Show your work.

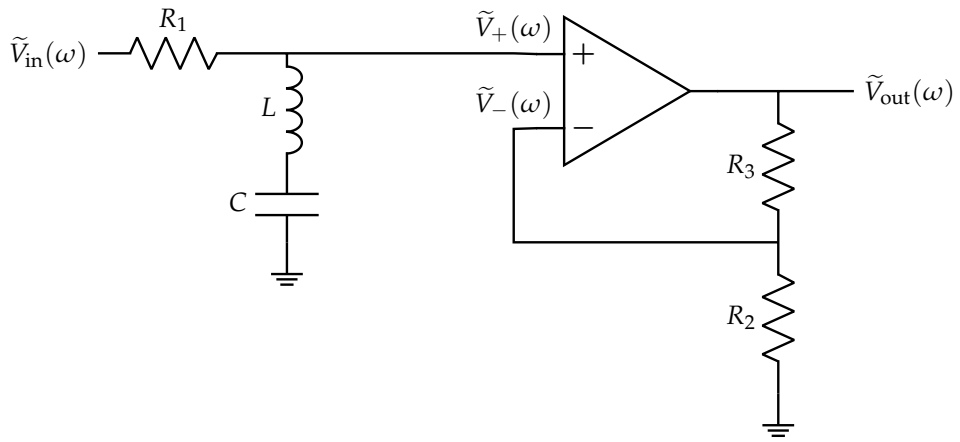

Figure 3: LC Notch filter and non-inverting amplifier

Solution:

i. The overall circuit in Fig 3 is the cascade of a voltage divider from $\widetilde{V}_{\text{in}}(\omega)$ to $\widetilde{V}_+(\omega)$ and a non-inverting amplifier from $\widetilde{V}_+(\omega)$ to $\widetilde{V}_{\text{out}}(\omega)$. The transfer function is derived as follows (op-amp in negative feedback implying $\widetilde{V}_+(\omega) = \widetilde{V}_-(\omega)$):

$$\frac{\widetilde{V}_+(\omega)}{\widetilde{V}_{\text{in}}(\omega)} = \frac{\text{j}\omega L + \frac{1}{\text{j}\omega C}}{R_1 + \text{j}\omega L + \frac{1}{\text{j}\omega C}} \tag{22}$$

$$= \frac{\text{j}\omega(L - \frac{1}{\omega^2 C})}{R_1 + \text{j}\omega(L - \frac{1}{\omega^2 C})} \tag{23}$$

$$\frac{\widetilde{V}_{\text{out}}(\omega)}{\widetilde{V}_+(\omega)} = \frac{\widetilde{V}_{\text{out}}(\omega)}{\widetilde{V}_-(\omega)} = \frac{R_2 + R_3}{R_2} \tag{24}$$

$$\implies H_{\text{notch}}(\omega) = \frac{\widetilde{V}_{\text{out}}(\omega)}{\widetilde{V}_{\text{in}}(\omega)} = \left(1 + \frac{R_3}{R_2}\right) \cdot \frac{\text{j}\omega(L - \frac{1}{\omega^2 C})}{R_1 + \text{j}\omega(L - \frac{1}{\omega^2 C})} \tag{25}$$

$$= \left(1 + \frac{R_3}{R_2}\right) \cdot \frac{1 - \omega^2 LC}{1 - \omega^2 LC + \text{j}\omega C R_1} \tag{26}$$

ii. We wish to place the notch at the noise frequency. The notch is at the frequency where the magnitude of the transfer function is 0, i.e. magnitude of the numerator is 0. Hence

$$|H_{\text{notch}}(\omega_{\text{noise}})| = 0 \tag{27}$$

$$\implies L - \frac{1}{\omega_{\text{noise}}^2 C} = 0 \tag{28}$$

$$\implies L = \frac{1}{\omega_{\text{noise}}^2 C} \tag{29}$$

$$= \frac{1}{1000^2 \times 0.5 \times 10^{-3}} = 2 \times 10^{-3} \tag{30}$$

Therefore the inductance is $L = 2\,\text{mH}$.

3. Transistor Behavior

For all NMOS devices in this problem, $V_{tn} = 0.5\text{V}$. For all PMOS devices in this problem, $|V_{tp}| = 0.6\text{V}$.

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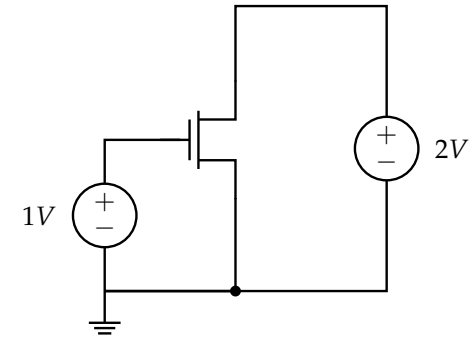
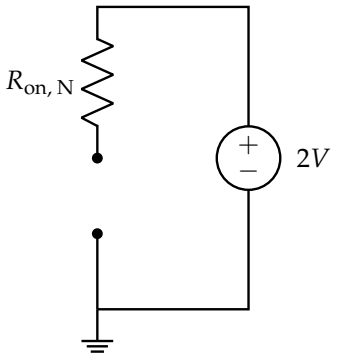
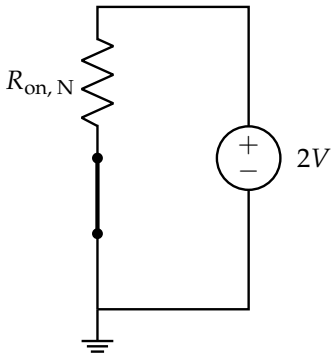
(a) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**





Circuit A

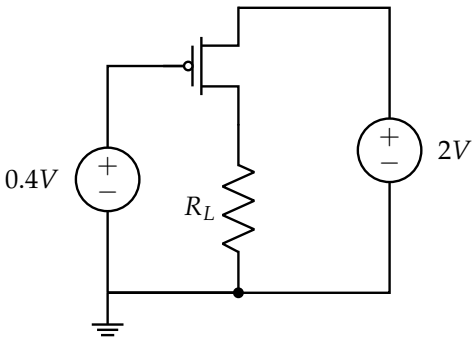


Circuit B

	A	B
Equivalent Circuit	◯	◯

Solution: For the NMOS, $V_{GS} = 1V > V_{tn} = 0.5V$, so the NMOS transistor is on. Thus circuit B is equivalent.

(b) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**



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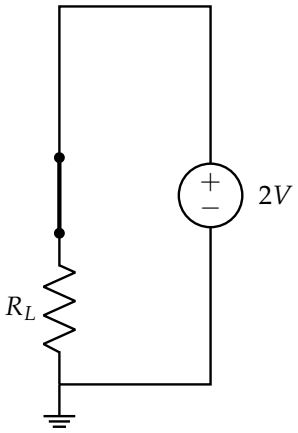
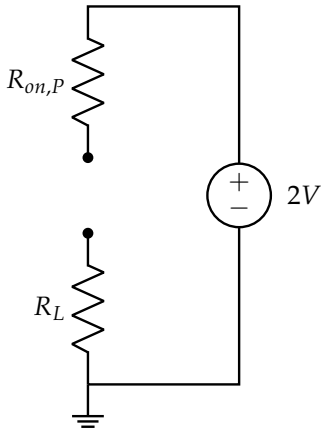
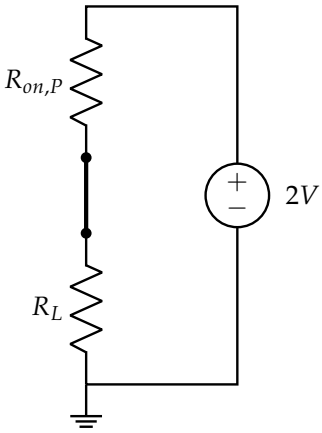


Circuit A



Circuit B

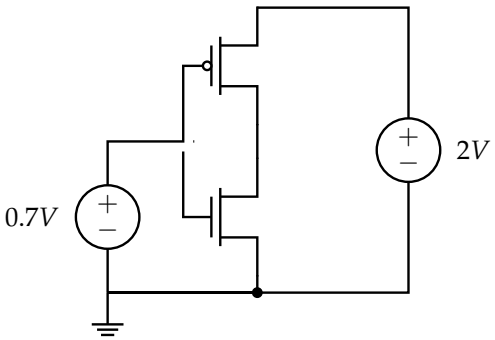


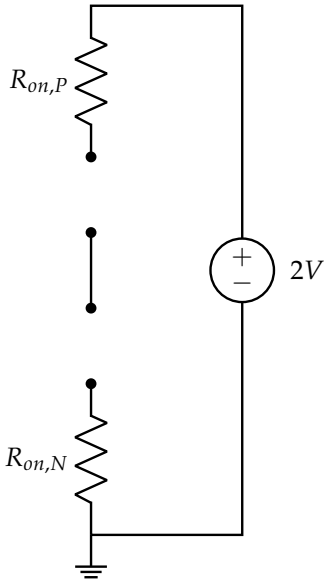
Circuit C

	A	B	C
Equivalent Circuit	◯	◯	◯

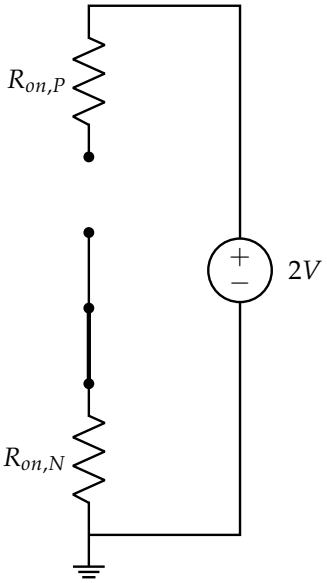
Solution: For the PMOS transistor, $|V_{GS}| = 1.6V > |V_{tp}| = 0.6V$, so the PMOS transistor is on. Thus circuit C is equivalent.

(c) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**

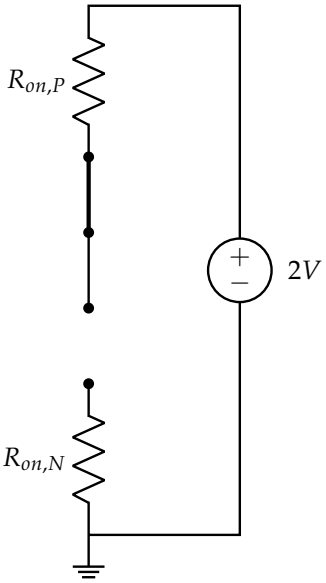




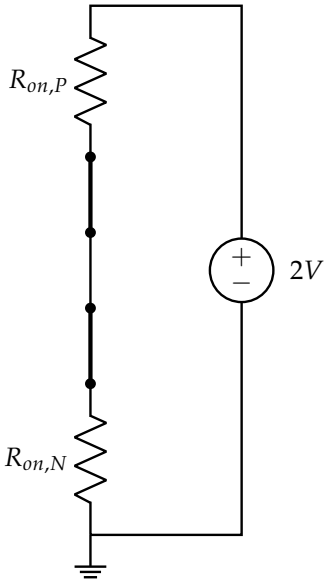
Circuit A



Circuit B



Circuit C



Circuit D

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	A	B	C	D
Equivalent Circuit	◯	◯	◯	◯

Solution: For the PMOS transistor, $|V_{GS}| = 1.3V > |V_{tp}| = 0.6V$, so the PMOS transistor is on. For the NMOS transistor, $V_{GS} = 0.7V > V_{tn} = 0.5V$, so the NMOS transistor is on. Note that in this case, both transistors are on. Thus circuit D is equivalent.

Aside:
In digital logic, it is usually undesirable to have this state in your system for several reasons. First, the output voltage of the inverter (the voltage at the shared drain of the NMOS and PMOS) will not be either 0 or VDD, which means the output voltage is not at 'true' binary value. In addition, we now have a direct current path through the NMOS and PMOS transistors from VDD to ground. This will burn a lot of power! In reality, all inverters briefly transition through this state where both NMOS and PMOS are on when the inputs change from 1 to 0 or 0 to 1.

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