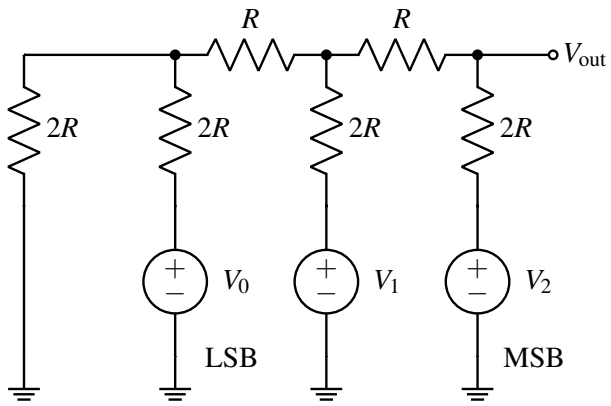
EECS 16B Designing Information Devices and Systems II
Spring 2021 UC Berkeley

Homework 2

This homework is due on Friday, January 29, 2021, at 11:00PM. Self-grades and HW Resubmission are due on Tuesday, February 2, 2021, at 11:00PM.

1. Digital-Analog Converter

A digital-analog converter (DAC) is a circuit for converting a digital representation of a number (binary) into a corresponding analog voltage. In this problem, we will consider a DAC made out of resistors only (resistive DAC) called the R-$2R$ ladder. Here is the circuit for a 3-bit resistive DAC.



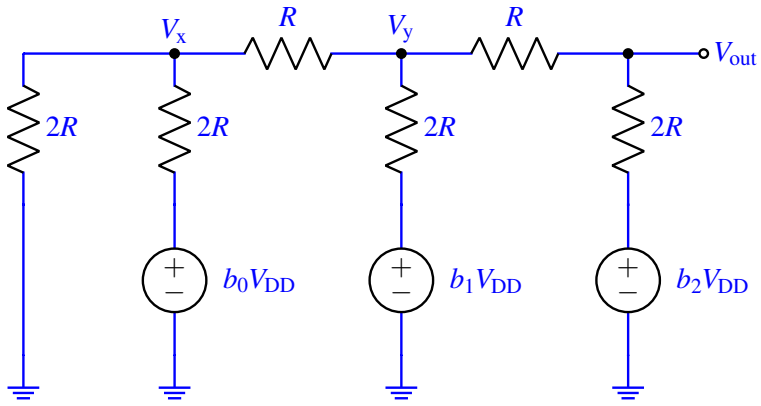
Let $b_0, b_1, b_2 = \{0, 1\}$ (that is, either 1 or 0), and let the voltage sources $V_0 = b_0 V_{\text{DD}}$, $V_1 = b_1 V_{\text{DD}}$, $V_2 = b_2 V_{\text{DD}}$, where V_{DD} is the supply voltage.

As you may have noticed, (b_2, b_1, b_0) represents a 3-bit binary (unsigned) number where each of b_i is a binary bit. b_0 is the least significant bit (LSB) and b_2 is the most significant bit (MSB). We will now analyze how this converter functions.

(a) If $b_2, b_1, b_0 = 1, 0, 0$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

There are several ways to solve this problem. For this solution set, we are going to solve for the generic solution rather than solve for each specific case of (a), (b), (c), and (d).



Applying KCL at nodes V_x, V_y, and V_{out}, we get

$$\frac{V_x}{2R} + \frac{V_x - b_0V_{DD}}{2R} + \frac{V_x - V_y}{R} = 0$$
$$\frac{V_y - b_1V_{DD}}{2R} + \frac{V_y - V_x}{R} + \frac{V_y - V_{out}}{R} = 0$$
$$\frac{V_{out} - b_2V_{DD}}{2R} + \frac{V_{out} - V_y}{R} = 0$$

Solving this system of equations using substitution or Gaussian elimination leads to

$$\frac{b_2V_{DD}}{2} + \frac{b_1V_{DD}}{4} + \frac{b_0V_{DD}}{8} = V_{out}$$

Plugging in 1, 0, 0 gives the answer.

$$V_{out} = \frac{V_{DD}}{2}$$

(b) If $b_2, b_1, b_0 = 0, 1, 0$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{out} = \frac{V_{DD}}{4}.$$

(c) If $b_2, b_1, b_0 = 0, 0, 1$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{out} = \frac{V_{DD}}{8}.$$

(d) If $b_2, b_1, b_0 = 1, 1, 1$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{out} = \frac{7V_{DD}}{8}.$$

(e) Finally, solve for V_{out} in terms of V_{DD} and the binary bits b_2, b_1, b_0.

Solution:

From part (a),

$$\frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}}.$$

(f) Explain how your results above show that the resistive DAC converts the 3-bit binary number (b_2, b_1, b_0) to the output analog voltage V_{out}.

Solution:

Every increment of $\frac{1}{8}V_{\text{DD}}$ on V_{DD} represents an increment of 1 to the 3-bit binary number $(b_2 b_1 b_0)$.

For example, if $V_{\text{out}} = \frac{5}{8}V_{\text{DD}}$, the input was 5 in binary (1 0 1)$\rightarrow$ ($b_2 = 1$ $b_1 = 0$ $b_0 = 1$).

2. Complex Numbers

A common way to visualize complex numbers is to use the complex plane. Recall that a complex number z is often represented in Cartesian form.

$$z = x + jy \text{ with } \text{Re}\{z\} = x \text{ and } \text{Im}\{z\} = y$$

See Figure 1 for a visualization of z in the complex plane.

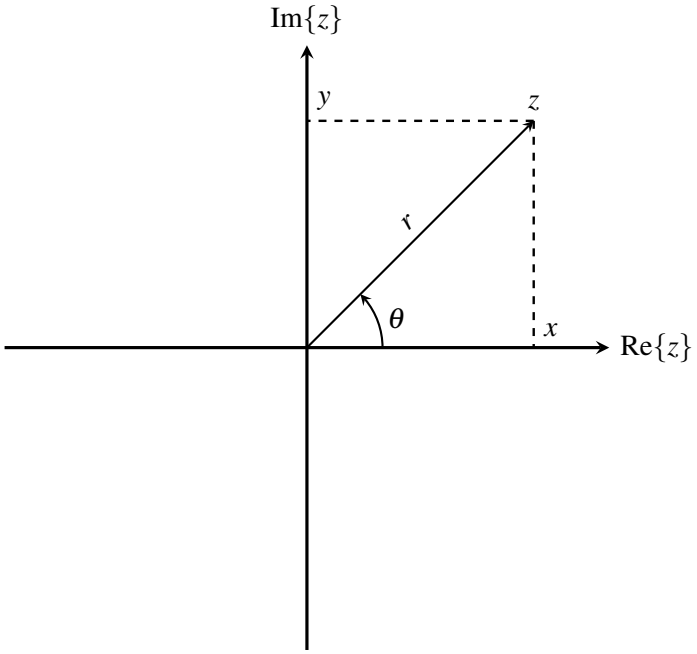


Figure 1: Complex Plane

In this question, we will derive the polar form of a complex number and use this form to make some interesting conclusions.

(a) **Calculate the length of z in terms of x and y as shown in Figure 1.** This is the magnitude of a complex number and is denoted by $|z|$ or r.
(Hint: Use the Pythagorean theorem.)
Solution:

$$r = \sqrt{x^2 + y^2} = |z|$$

(b) **Represent x, the real part of z, and y, the imaginary part of z, in terms of r and θ.**
Solution:

$$x = r\cos(\theta) \text{ and } y = r\sin(\theta)$$

(c) **Substitute for x and y in z.** Use Euler's identity[1] $e^{j\theta} = \cos\theta + j\sin\theta$ to **conclude that,**

$$z = re^{j\theta}.$$

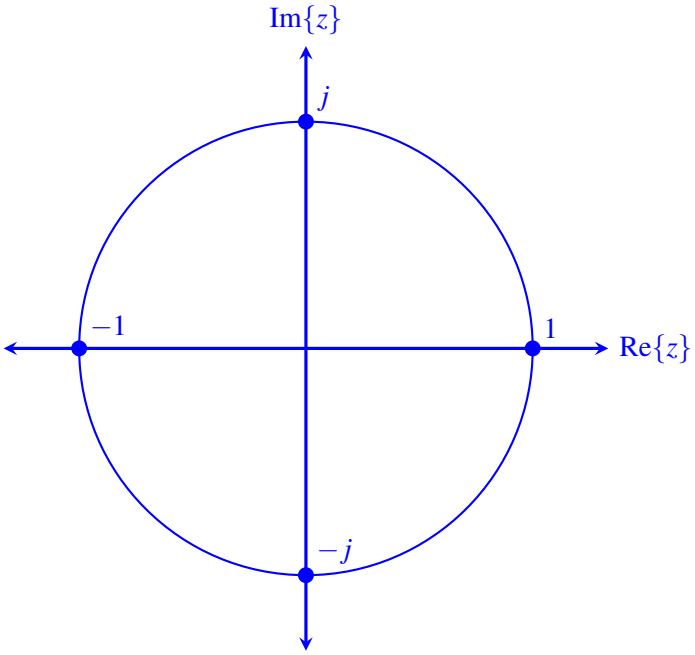
[1] also known as de Moivre's Theorem.

Solution:

$$\begin{aligned} z &= r\cos(\theta) + jr\sin(\theta) \\ &= r(\cos(\theta) + j\sin(\theta)) \\ &= re^{j\theta} \end{aligned}$$

(d) In the complex plane, **sketch the set of all the complex numbers such that** $|z| = 1$. **What are the** z **values where the sketched figure intersects the real axis and the imaginary axis?**

Solution:



(e) If $z = re^{j\theta}$, **prove that** $\bar{z} = re^{-j\theta}$. Recall that the complex conjugate of a complex number $z = x + jy$ is $\bar{z} = x - jy$.

Solution:

$$\begin{aligned} \bar{z} &= \overline{(r(\cos(\theta) + j\sin(\theta)))} \\ &= r(\cos(\theta) - j\sin(\theta)) \\ &= r(\cos(-\theta) + j\sin(-\theta)) \\ &= re^{-j\theta} \end{aligned}$$

(f) **Show (by direct calculation) that,**

$$r^2 = z\bar{z}.$$

Solution:

$$z\bar{z} = re^{j\theta}re^{-j\theta} = r^2e^{j\theta - j\theta} = r^2e^0 = r^2$$

3. Existence and uniqueness of solutions to differential equations

Let's show that if any function x satisfies

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \alpha x(t) \tag{1}$$

as well as

$$x(0) = x_0, \tag{2}$$

then it is unique: if y is *any function* that meets these two criteria then $x = y$.

In order to do this, we will first verify that a solution exists. Then we will compare it to a hypothetical alternative solution—and our goal will to be establish that these two solutions are equal.

(a) **Verify that $x_d(t) = x_0 e^{\alpha t}$ satisfies (1) and (2).** (For this proof, x_d will be the "reference solution" against which alternates will be compared.)

Solution: Taking the derivative of $x_d(t)$ with respect to t gives $\alpha x_0 e^{\alpha t}$ by the chain rule, and this is equal to $\alpha x_d(t)$ by inspection. So (1) is satisfied.
Evaluating $x_d(0) = x_0 e^{\alpha \cdot 0} = x_0$ and so (2) is also satisfied.

(b) To show that this solution is in fact unique, we need to consider a hypothetical $y(t)$ that also satisfies (1) and (2).

Our goal is to show that $y(t) = x(t)$ for all $t \geq 0$. (The domain $t \geq 0$ is where we have defined the conditions (1) and (2). Outside of that domain, we don't have any constraints.)

How can we show that two things are equal? In the past, you have probably shown that two quantities or functions are equal by starting with one of them, and then manipulating the expression for it using valid substitutions and simplifications until you get the expression for the other one. However, here, we don't have an expression for $y(t)$ so that style of approach won't work.

In such cases, we basically have a couple of basic ways of showing that two things are the same.

- Take the difference of them, and somehow argue that it is 0.
- Take the ratio of them, and somehow argue that it is 1.

We will follow the ratio approach in this problem. First assume that $x_0 \neq 0$. In this case, we are free to define $z(t) = \frac{y(t)}{x_d(t)}$ since we are dividing by something other than zero.

What is $z(0)$?

Solution:
We know $z(0) = \frac{y(0)}{x_d(0)} = \frac{x_0}{x_0} = 1$ since $y(0) = x_0$ by (2) and plugging in 0 for t into the exact expression for $x_d(t)$.

(c) **Take the derivative $\frac{d}{dt}z(t)$ and simplify using (1) and what you know about the derivative of $x_d(t)$.** *(HINT: The quotient rule for differentiation might be helpful since a ratio is involved.)*

Solution:
The quotient rule tells us how to take the derivative of $\frac{y}{x_d}$ (we can also view this using the product rule, which is also just another manifestation of the chain rule for differentiation in the multivariate case). The rule applies because the functions involved are differentiable by definition and the denominator is nonzero.

$$\frac{d}{dt}z(t) = \frac{d}{dt}\frac{y(t)}{x_d(t)} = \frac{\frac{d}{dt}y(t)x_d(t) - y(t)\frac{d}{dt}x_d(t)}{(x_d(t))^2} \tag{3}$$

$$= \frac{\alpha y(t)x_d(t) - y(t)\alpha x_d(t)}{(x_d(t))^2} \tag{4}$$

$$= \frac{0}{(x_d(t))^2} = 0 \tag{5}$$

Notice that here, what is important is that both y and x_d satisfy (1) and so the numerator in the quotient rule cancels out to zero. The details of $x_d(t)$ didn't end up mattering.

You should see that this derivative is always 0 and hence $z(t)$ does not change. **What does that imply for y and x_d ?**

Solution: Since $z(t)$ has zero derivative, it cannot change, and hence it stays at its initial value, which is 1. So it is always 1 and hence $\frac{y(t)}{x_d(t)} = 1$ so $y(t) = x_d(t)$.

(d) At this point, we have shown uniqueness in most cases. Just one special case is left: $x_0 = 0$. The ratio technique omitted this case, because as $x_d(t) = 0$, x_d cannot be the denominator of a fraction.

To complete our proof we must show that if $x_0 = 0$, then $y(t) = 0$ for all t, and we will do so by assuming that $y(t)$ is not identically 0 for $t > 0$—that is, at some $t_0 > 0$ $y(t_0) = k \neq 0$.

From (2), we know that $y(0) = 0$. In the subsequent sub parts, we will try to work backwards in time from the point $t = t_0$ to $t = 0$ and conclude that y violates (2) if $y(t_0) \neq 0$.

Apply the change of variables $t = t_0 - \tau$ to (1) to get a new differential equation for $\widetilde{x}(\tau) = x(t_0 - \tau)$ that specifies how $\frac{d}{d\tau}\widetilde{x}(\tau)$ must relate to $\widetilde{x}(\tau)$. This should hold for $-\infty < \tau \leq t_0$.

Solution:

$$\frac{d}{d\tau}\widetilde{x}(\tau) = \frac{d}{d\tau}x(t_0 - \tau) \tag{6}$$

$$= -\alpha x(t_0 - \tau) \tag{7}$$

$$= -\alpha\widetilde{x}(\tau) \tag{8}$$

where the second line used the chain rule for differentiation and (1).

This holds for all $t \geq 0$ which means $t_0 - \tau \geq 0$ which is the same as $\tau \leq t_0$.

(e) Because the previous part resulted in a differential equation of a form for which we have already proved uniqueness for the case of nonzero initial condition, and since $\widetilde{y}(0) = y(t_0) = k \neq 0$, we know what $\widetilde{y}(\tau)$ must be. **Write the expressions for $\widetilde{y}(\tau)$ for $\tau \in [0, t_0]$ and what that implies for $y(t)$ for $t \in [0, t_0]$.**

Solution: We know that $\widetilde{y}$ satisfies $\frac{d}{d\tau}\widetilde{y}(\tau) = -\alpha\widetilde{y}(\tau)$ and that $\widetilde{y}(0) = k \neq 0$. Consequently, by the uniqueness theorem already proved, we know that it must be the case that $\widetilde{y}(\tau) = ke^{-\alpha\tau}$ for the range $\tau > 0$ as long as the differential equation is valid.

This means that $y(t) = ke^{-\alpha(t_0 - t)}$ as long as $0 \leq t \leq t_0$.

(f) **Evaluate $y(0)$ and argue that this is a contradiction for the specified initial condition (2).**

Solution:

Evaluating this expression at $t = 0$ gives $y(0) = ke^{-\alpha t_0}$. Because $k \neq 0$, this means $y(0) \neq 0$. This is a contradiction with (2) since that asserts a zero initial condition $x_0 = 0$.

Consequently, such a $y(t)$ cannot exist and only the all zero solution is permitted — establishing uniqueness in this case of $x_0 = 0$ as well.

(g) Explain in your own words why it matters that solutions to these differential equations are unique.

Solution:

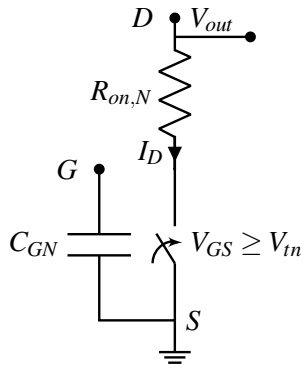
Uniqueness means that we need not continue looking once a satisfactory guess has been reached. If our model had non-unique solutions—such as kinematics problem where the quantity of interest arises as a root of a quadratic—then we would potentially have to choose between multiple, or even infinitely many solutions.

Although we gave you lots of guidance in this problem, we hope that you can internalize this way of thinking.

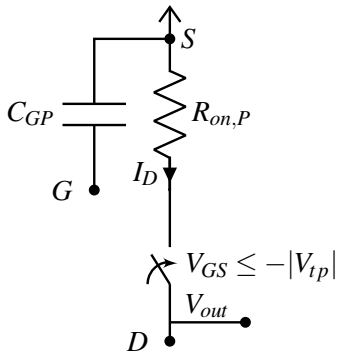
This elementary approach to proving the uniqueness of solutions to differential equations works for the kinds of linear differential equations that we will tend to encounter in EECS16B. For more complicated nonlinear differential equations, further conditions are required for uniqueness (appropriate continuity and differentiability) and proofs can be found in upper-division mathematics courses on differential equations when you study the Picard-Lindelöf theorem. (It involves looking at the magnitude of the difference of the two hypothetical solutions and showing this has to be arbitrarily small and hence zero. However, the basic elementary case we have established here can be viewed as a building block — the quotient rule gets invoked in the appropriate place, etc. The additional ingredients that are out-of-scope for lower-division courses are fixed-point theorems — which you can think of as more general siblings of the intermediate-value theorem you saw in basic calculus.)

4. Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



a NMOS Transistor Resistor-switch-capacitor model



b PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on,N} = R_{on,P} = 1$ kΩ, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1$fF (femto-Farads = 10^{-15}). We assume the "off resistance" (the resistance when the transistor is off) is infinite (*i.e.*, the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 3).

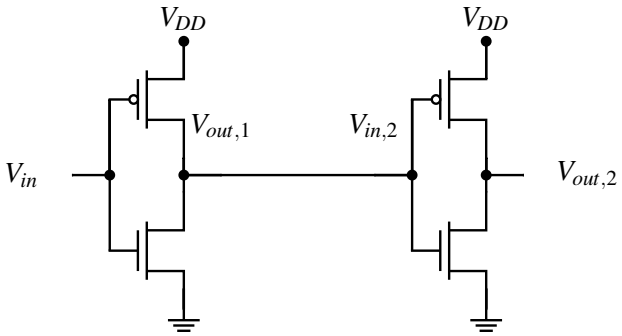


Figure 3: CMOS Inverter chain

(a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,1}$) for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

Solution:

To analyze this circuit as an RC circuit we can recall the transistor switch model. Using this we can see that the first inverter's output appears as a resistor connected to V_{DD} when the input is low (nmos off, pmos on), or a resistor connected to ground when the input turns high (nmos on, pmos off).

Before $t = 0$, the input to the first inverter was low for a long time. This means that for $t < 0$, the output of the inverter ($V_{out,1}$) had been held at V_{DD} for a long time.

At $t = 0$, the input goes high, which means that the input inverter's nmos device turns on, connecting $V_{out,1}$ to ground through a resistance of R_{on}.

The second inverter "loads" the output of the first inverter. From the notes in the problem, we can model the gates of the transistors as capacitors. These gates together form our capacitive load. The gate of the pmos acts as a capacitor to V_{DD} and the gate of the nmos acts as a capacitor to ground.

Using this we can draw the following RC circuit:

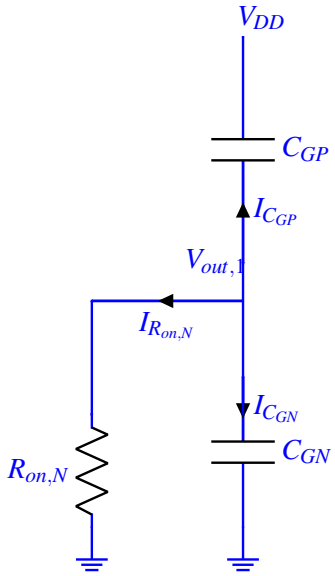


Figure 4: First inverter output at 0

To get the differential equation describing the output of the first inverter at time $t \geq 0$ let us first think about the behavior of the circuit at and after $t = 0$.

Before $t = 0$ we know that the output $V_{out,1} = V_{DD}$. This means that C_{GN} is charged, while C_{GP} is not as there is no voltage difference across it.

At $t = 0$, when the input to the first inverter changes (input switches to high), the nmos will turn on, discharging the $V_{out,1}$ node. Thus $V_{out,1}$ will eventually discharge to zero in steady state.

We know the voltage across C_{GP} is $V_{out,1}(t) - V_{DD}$ and the voltage across C_{GN} is $V_{out,1}(t)$. Using this information we can set up a differential equation to solve for $V_{out}(t)$:

$$I_{C_{GP}} = C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \tag{9}$$

$$I_{C_{GN}} = C_{GN}\frac{d}{dt}V_{out,1}(t) \tag{10}$$

$$I_{R_{on,N}} = \frac{V_{out,1}(t)}{R_{on,N}} \tag{11}$$

$$I_{C_{GP}} + I_{C_{GN}} = -I_{R_{on,N}} \tag{12}$$

$$C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{GN}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on,N}} \tag{13}$$

$$C_{GP}\frac{d}{dt}V_{out,1}(t) + C_{GN}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on,N}} \tag{14}$$

$$(C_{GP} + C_{GN})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on,N}} \tag{15}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on,N}(C_{GP} + C_{GN})} \tag{16}$$

(b) Given the initial conditions in part (a), **solve for $V_{out,1}(t)$.**

Solution: We know that the solution to a differential equation of the form

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}}{R_{on,N}(C_{GP} + C_{GN})}$$

is

$$V_{out,1}(t) = ke^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}$$

Plugging in the initial condition $V_{out,1}(0) = V_{DD}$ we find that $V_{out,1}(t) = V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}$.

(c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

Solution:

(1) We know that the output of our inverter started with the initial value V_{DD}.

(2) Since the differential equation tells us the change in value of $V_{out,1}(t)$ at time t we can simply plug in $t = 0$ into our differential equation to get the initial slope:

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(0)}{R_{on,N}(C_{GP} + C_{GN})} \tag{17}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{DD}}{R_{on,N}(C_{GP} + C_{GN})} \tag{18}$$

Thus the initial slope is $-\frac{V_{DD}}{R_{on,N}(C_{GP}+C_{GN})}$

(3) Since the input to the inverter changed from low to high we know the output of the first inverter ($V_{out,1}$) is going to go to 0 in steady state, as this node will be discharged by the first inverter's nmos

transistor.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD} e^{-\frac{\infty}{R_{on,N}(C_{GP}+C_{GN})}} = 0$.
(4) To approximate when the output will decay to $\frac{1}{3}$ its original value, we use the fact that $e^{-1} = \frac{1}{e} \approx \frac{1}{3}$. We thus want to find when $V_{out,1} = V_{DD} e^{-1}$. This will occur when the e term is raised to -1, which occurs when $t = R_{on,N}(C_{GP} + C_{GN}) = 2 * 10^{-12}$.

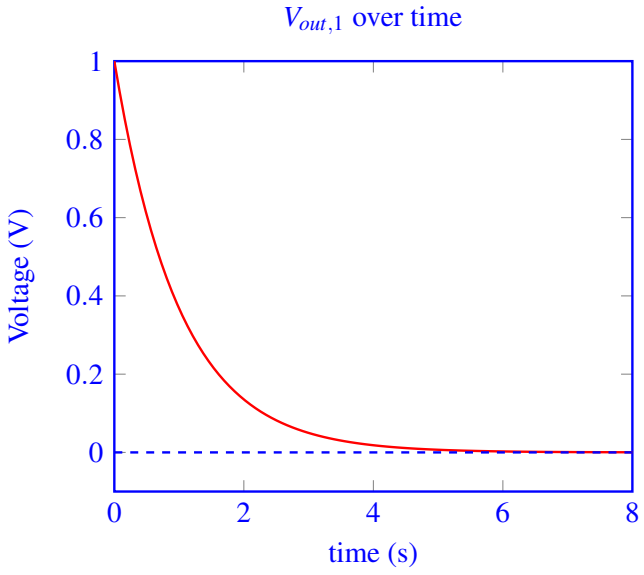


Figure 5

(d) A long time later, the input to the first inverter switches low again.
Solve for $V_{out,1}(t)$.
Sketch the output voltage of the first inverter ($V_{out,1}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.

Solution:

We know that after a long time, the output of the first inverter has stabilized to 0. When the input switches low again, the input inverter's nmos device turns off, while the input inverter's pmos device turns on. This connects the $V_{out,1}$ node to V_{DD}, as shown in Figure 6.

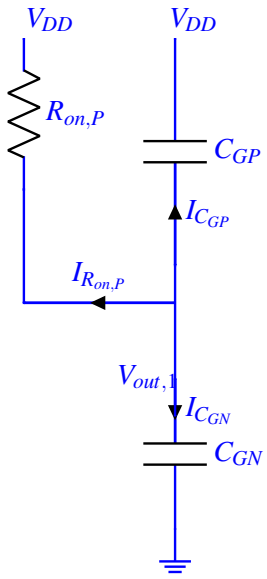


Figure 6: Inverter output at 1

To set up the differential equation, we apply KVL and KCL again:

$$I_{C_{GP}} = C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \tag{19}$$

$$I_{C_{GN}} = C_{GN}\frac{d}{dt}V_{out,1}(t) \tag{20}$$

$$I_{R_{on,P}} = \frac{V_{out,1}(t) - V_{DD}}{R_{on,P}} \tag{21}$$

$$I_{C_{GP}} + I_{C_{GN}} = -I_{R_{on,P}} \tag{22}$$

$$C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{GN}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on,P}} \tag{23}$$

$$C_{GP}\frac{d}{dt}V_{out,1}(t) + C_{GN}\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on,P}} \tag{24}$$

$$(C_{GP} + C_{GN})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on,P}} \tag{25}$$

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on,P}(C_{GP} + C_{GN})} \tag{26}$$

We will use substitution of variables:

$$x(t) = V_{out,1}(t) - V_{DD} \tag{27}$$

$$V_{out,1}(t) = x(t) + V_{DD} \tag{28}$$

$$\frac{d}{dt}x(t) = \frac{d}{dt}V_{out,1}(t) \tag{29}$$

Substituting in:

$$\frac{d}{dt}x(t) = -\frac{x}{R_{on,P}(C_{GP} + C_{GN})} \tag{30}$$

$$x(t) = Ae^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}} \tag{31}$$

Substituting again for $x(t)$:

$$V_{out,1}(t) = V_{DD} + Ae^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}$$

Using the initial condition $V_{out,1} = 0$ (as the input to the first inverter was high for a long time before switching low) implies $A = -V_{DD}$. Thus:

$$V_{out,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}\right)$$

(1) Because the input to the first inverter was high for a long time, we know the initial value of $V_{out,1}(t) = 0$. This was the initial condition applied to the solution of the differential equation, above.

(2) To find the initial value of the slope we can plug in $t = 0$ to the above differential equation:

$$\frac{d}{dt}V_{out,1}(t) = \frac{(V_{DD} - V_{out,1}(0))}{R_{on,P}(C_{GP}+C_{GN})}$$

where $V_{out,1}(0) = 0$. Thus our initial slope is $\frac{(V_{DD})}{R_{on,P}(C_{GP}+C_{GN})}$. Notice this slope is positive while the previous part had a negative slope.

(3) Since the input to the inverter changed from low to high and the input inverter's pmos is now on, we know the output of the first inverter is going to go to V_{DD} in steady state.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD}\left(1 - e^{-\frac{\infty}{R_{on,P}(C_{GP}+C_{GN})}}\right) = V_{DD}(1-0) = V_{DD}$.

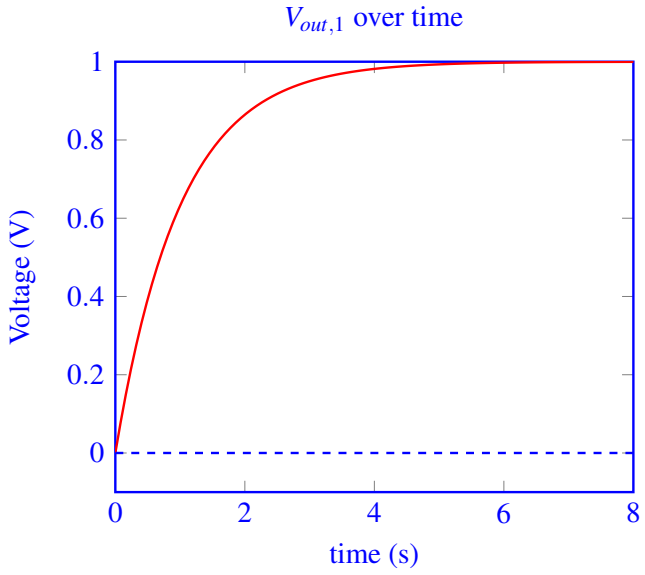


Figure 7

(e) For each complete input cycle described above ($V_{in} = 0\text{V} \rightarrow 1\text{V} \rightarrow 0\text{V}$), **how much charge is pulled out of the power supply?** Give both a symbolic and numerical answer. **Consider only the charge needed to charge up the $V_{out,1}$ node.**

Solution:

To find the charge required from the supply, we can integrate the current required from the supply during each phase of the cycle ($Q = \int_0^\infty I_{V_{DD}}(t)dt$).

During the input step from $V_{in} = 0$ to $V_{in} = V_{DD}$, we know that the voltage is $V_{out,1}(t) = V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}$. We then get:

$$\begin{aligned} I_{V_{DD}} = I_{C_{GP}} &= C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \\ &= C_{GP}\frac{-1}{R_{on,N}(C_{GP}+C_{GN})}V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}} \end{aligned}$$

Thus:

$$\begin{aligned} Q_{0\rightarrow 1} &= \int_0^\infty I_{C_{GP}}(t)dt = \int_0^\infty C_{GP}\frac{-1}{R_{on,N}(C_{GP}+C_{GN})}V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}dt \\ &= C_{GP}\cdot V_{DD}e^{-\frac{t}{R_{on,N}(C_{GP}+C_{GN})}}\Big|_0^\infty \\ &= C_{GP}\cdot V_{DD}(0-1) = -C_{GP}\cdot V_{DD} \end{aligned}$$

During the input step from $V_{in} = V_{DD}$ to $V_{in} = 0$, we know that the voltage is $V_{out,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}\right)$. The current from the supply will be equal to the sum of the resistor current and PMOS gate capacitor current: $I_{V_{DD}} = I_R + I_{C_{GP}}$. We get:

$$\begin{aligned} I_{V_{DD}} = I_{C_{GP}} + I_R &= C_{GP}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + \frac{V_{out,1}(t) - V_{DD}}{R_{on,P}} \\ &= -C_{GP}\frac{-1}{R_{on,P}(C_{GP}+C_{GN})}V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}} + \frac{V_{DD}\left(1 - e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}\right) - V_{DD}}{R_{on,P}} \\ &= -C_{GP}\frac{-1}{R_{on,P}(C_{GP}+C_{GN})}V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}} + \frac{-V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}}{R_{on,P}} \end{aligned}$$

Thus:

$$\begin{aligned} Q_{1\rightarrow 0} &= \int_0^\infty I_{C_{GP}}(t) + I_R(t)dt = \int_0^\infty -C_{GP}\frac{-1}{R_{on,P}(C_{GP}+C_{GN})}V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}} + \frac{-V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}}{R_{on,P}}dt \\ &= -C_{GP}V_{DD}e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}\Big|_0^\infty + \frac{-V_{DD}}{R_{on,P}}\cdot -1\cdot R_{on,P}(C_{GP}+C_{GN})e^{-\frac{t}{R_{on,P}(C_{GP}+C_{GN})}}\Big|_0^\infty \\ &= -C_{GP}V_{DD}(0-1) + (C_{GP}+C_{GN})V_{DD}(0-1) \\ &= -C_{GN}V_{DD} \end{aligned}$$

The total charge is thus

$$Q_{total} = Q_{0\to1} + Q_{1\to0} = -C_{GP}V_{DD} - C_{GN}V_{DD} = -(C_{GP} + C_{GN})V_{DD}$$

Note that the current direction for $I_{V_{DD}}$ was pointing into the V_{DD} source, so the charge represents the charge moved **into** the power supply. As the question asks for the charge pulled out of the power supply, we know:

$$Q_{\text{pulled out of power supply}} = -Q_{total} = (C_{GP} + C_{GN})V_{DD} = (1\text{fF} + 1\text{fF}) \cdot 1\text{V} = 2\text{fC}$$

Alternative solution:
During the input step when V_{in} switches from V_{DD} to 0, note that $V_{out,1}$ is connected to V_{DD} through the input inverter's PMOS. Thus, during this phase, C_{GN} is charging while C_{GP} is discharging. We use the equation

$$Q = CV$$

noting that $V_{initial} = 0$ and $V_{final} = V_{DD}$.
Thus:

$$\begin{aligned} Q_{1\to0} &= CV \\ &= C_{GN}(V_{DD} - 0) \\ &= C_{GN}V_{DD} \\ &= 1\text{fF} \cdot 1\text{V} = 1\text{fC} \end{aligned}$$

During the input step when V_{in} switches from 0 to V_{DD}, note that $V_{out,1}$ is connected to ground through the input inverter's NMOS. In this case, C_{GN} is discharging while C_{GP} is charging.
Thus:

$$\begin{aligned} Q_{0\to1} &= CV \\ &= C_{GP}(V_{DD} - 0) \\ &= C_{GP}V_{DD} \\ &= 1\text{fF} \cdot 1\text{V} = 1\text{fC} \end{aligned}$$

For the entire input cycle, we thus find that $Q = (C_{GN} + C_{GP})V_{DD} = 2\text{fC}$.

5. Group formation survey

Participating in study groups is completely optional. In the following survey, please choose an option that is best for you. Note that submitting this form is required to get full credit for this HW question.

Group Formation Survey - Google Form

6. Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student!
We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

(a) **What sources (if any) did you use as you worked through the homework?**

(b) **If you worked with someone on this homework, who did you work with?**
List names and student ID's. (In case of homework party, you can also just describe the group.)

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