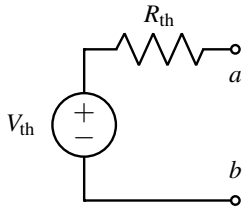
EECS 16B Designing Information Devices and Systems II
Spring 2021 Discussion Worksheet

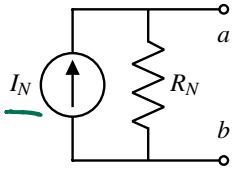
# Discussion 2A

## 1 Circuit Equivalence

To review the circuit equivalence concepts exercised in this worksheet, please see Note 0B, adapted from the EECS 16A Course Notes. We will work through examples in this worksheet. The two forms are presented below for your reference.

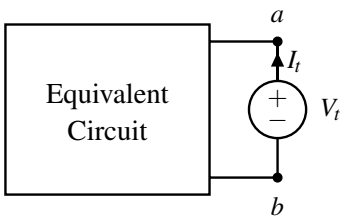



(a) General form of a Thévenin equivalent circuit. Given a circuit and two output terminals, we know the above gives a voltage-source based equivalent; the work lies in solving for $V_{th}$ and $R_{th}$.

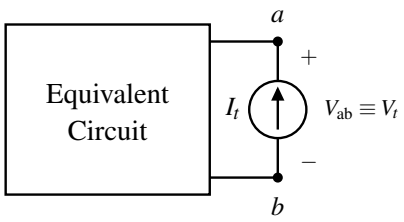



(b) General form of a Norton equivalent circuit, the current-source based equivalent form for a given circuit. Here, we must solve for $I_N$ and $R_N$.

Below, we display pictorially how to apply current or voltage test sources to a circuit to find $R_{eq}$.




(a) By applying a test voltage $V_t$ across $a$ and $b$, we can measure the resulting current draw of the equivalent circuit $I_t$ and use that to calculate $R_{eq}$.




(b) By feeding a test current $I_x$ into the equivalent circuit, we can measure the resulting voltage drop $V_{ab}$ and calculate $R_{eq}$.

Figure 2: We can use either a test voltage source or a test current source to find $R_{eq}$. The choice for what is easier will depend on the specific problem.

## 2 Transistor Introduction

Transistors (as presented in this course) are 3 terminal, voltage-controlled switches. This means that, when a transistor is "on," the Source (S) and Drain (D) terminals are connected via a low resistance path (short circuit). When a transistor is "off," the Source and Drain terminals are disconnected (open circuit).

Two common types of transistors are NMOS and PMOS transistors. Their states (shorted or open) are determined by comparing the voltage between the $G$ and $S$ terminals ($V_{GS} = V_G - V_S$) to a "threshold voltage"

($V_{tn}$ for NMOS, $V_{tp}$ for PMOS). Generally, NMOS transistors turn on when $V_{GS}$ is high enough, and PMOS transistors turn on when $V_{GS}$ is low enough (they have complementary behavior!). Transistors are extremely useful in digital logic design since we can use them to implement Boolean logic operators.

In this class, $V_{tn}$ denotes how much **higher** $V_G$ needs to be relative to $V_S$ for the NMOS to be on (allow current flow from drain to source), and $|V_{tp}|$ denotes how much **lower** $V_G$ gate needs to be relative to $V_S$ for the PMOS to be on.

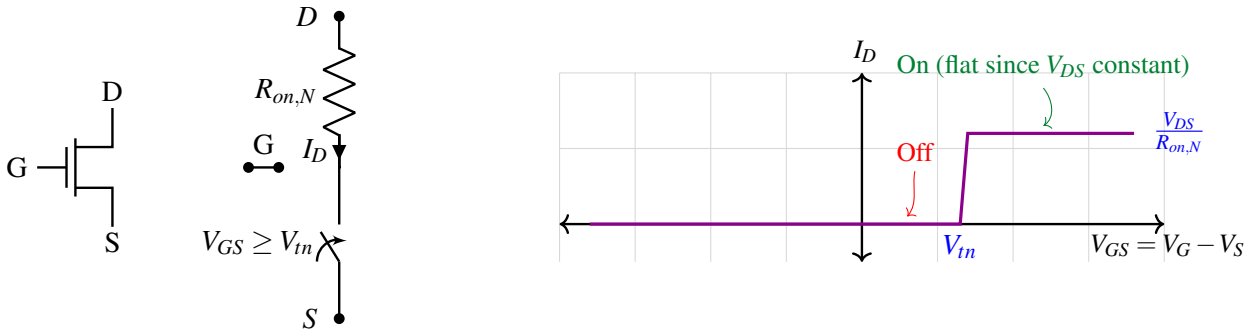



Figure 3: NMOS Transistor Resistor-switch model (the current holding constant at high $V_{GS}$ assumes that $V_{DS}$ is constant).

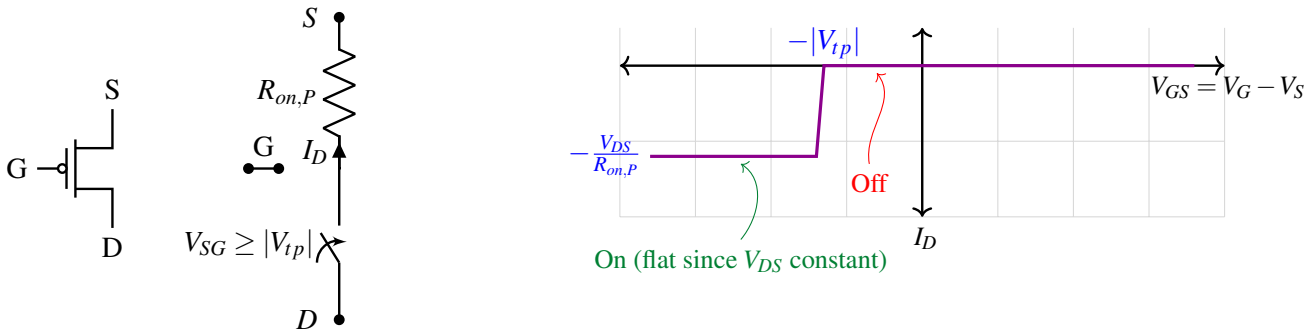



Figure 4: PMOS Transistor Resistor-switch model (the current holding constant at low $V_{GS}$ assumes that $V_{DS}$ is constant). Note that $V_{SG} = -V_{GS}$.

We mentioned that transistors can be connected to perform boolean algebra. An example of this is seen in Section 2, which is called an "inverter" and represents a NOT gate.

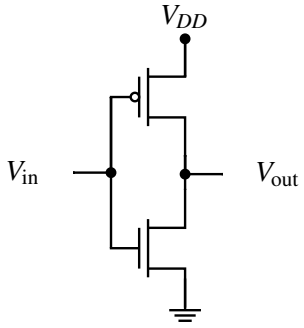



Figure 5: CMOS Inverter

To see why this circuit is called an inverter, we consider the following cases[1]:

(1) **The input is high**: $V_{\text{in}} = V_{DD}$. Then, since $V_{GS} \geq V_{tn}$ ($V_{\text{in}} \geq V_{tn}$), the NMOS is on. Also, since $V_{GS} \geq V_{tp}$ ($V_{\text{in}} - V_{DD} \geq V_{tp} \implies V_{\text{in}} \geq V_{DD} - |V_{tp}|$), the PMOS is off. So, only the NMOS switch is closed, and $V_{\text{out}} = 0$. That is, **the output is low**.

(2) **The input is low**: $V_{\text{in}} = 0$. Then, since $V_{GS} \leq V_{tn}$ ($V_{\text{in}} \leq V_{tn}$), the NMOS is off. Also, since $V_{GS} \leq V_{tp}$ ($V_{\text{in}} \leq V_{DD} - |V_{tp}|$), the PMOS is off. So, only the PMOS switch is closed, and $V_{\text{out}} = V_{DD}$. That is, **the output is high**.

We can summarize this analysis, using the following truth table:

| $V_{\text{in}}$ | $V_{\text{out}}$ | NMOS | PMOS |
|---|---|---|---|
| $V_{DD}$ | 0 | on | off |
| 0 | $V_{DD}$ | off | on |

If you think of $V_{DD}$ being a logical 1 and 0V being a logical 0, we have just created the most elementary logical operation using transistors!

Motivation for Equivalent Circuits:
→ simplify large circuits (group into functional blocks)
→ analyze significant/common blocks once and (potentially) reuse the equivalent model.

Motivation for understanding Transistors:
→ arguably the most fundamental block in digital logic
→ forms basis of computing; understand transistors ⟹ get ideas to design more efficient devices!

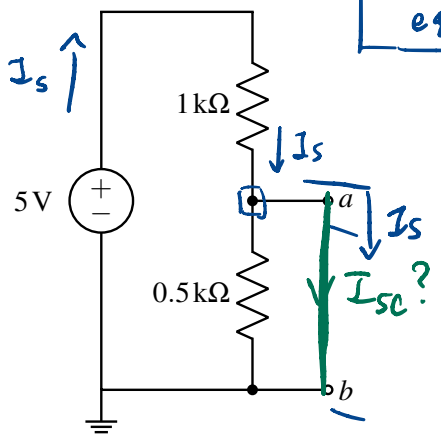
[1] When working with digital circuits like in Section 2, we usually only consider the values of $V_{\text{in}} = 0$ and $V_{\text{in}} = V_{DD}$.

## 1. Thévenin and Norton Equivalence

Find the Thévenin and Norton equivalents across terminals *a* and *b* for the circuits given below. Note that the general forms of these equivalents can be found in Figure 1a and Figure 1b.

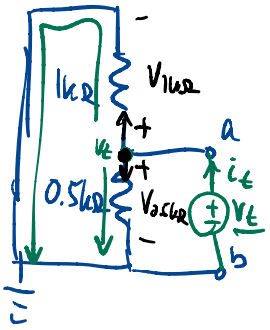
(a)

current-divider equation




$R_{TH}$

wire ⇔ zeroed voltage source




KCL

$I_t = I_{R,1k\Omega} + I_{R,0.5k\Omega}$

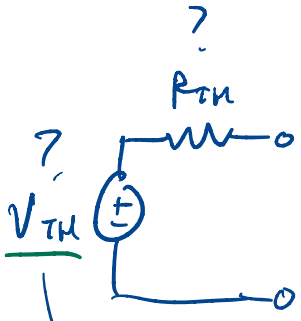
$I_t = \frac{V_{R,1k\Omega}}{1k\Omega} + \frac{V_{R,0.5k\Omega}}{0.5k\Omega}$ ($V_t$ over each)

$R_{eq} = 333\,\Omega$

$I_t \cdot 1k\Omega \cdot 0.5k\Omega = 0.5k\Omega \cdot V_{R,1k\Omega} + 1k\Omega \cdot V_{R,0.5k\Omega}$

$I_t \left( \frac{1k\Omega \cdot 0.5k\Omega}{1k\Omega + 0.5k\Omega} \right) = V_t$

$\frac{1k\Omega \cdot 0.5k\Omega}{1k\Omega + 0.5k\Omega} = \frac{V_t}{I_t}$

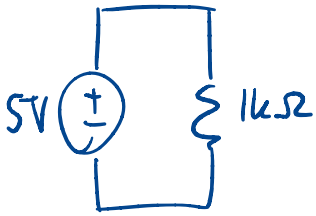



$V_{OC} = V_S \cdot \frac{R_2}{R_1 + R_2}$

$= 5V \cdot \frac{0.5k\Omega}{(0.5+1)k\Omega}$

$V_{OC} = 1.67V = V_{TH}$

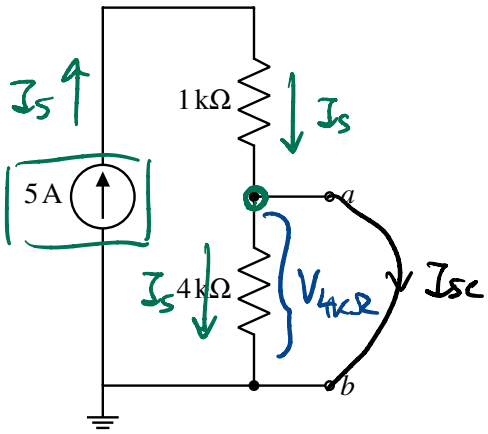
$I_N$:




$I_N = \frac{5V}{1k\Omega} = 5mA = I_{SC}$

($I_{SC}$ is all of $I_S$, because the 0.5kΩ resistor is shorted out).

(b)




$V_{TH}$: $V_{TH} = V_{4k\Omega}$

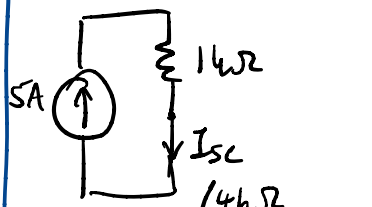
$V_{TH} = V_{4k\Omega} = I_S \cdot 4k\Omega$

$= 5A \cdot 4k\Omega$

$V_{TH} = 20kV$

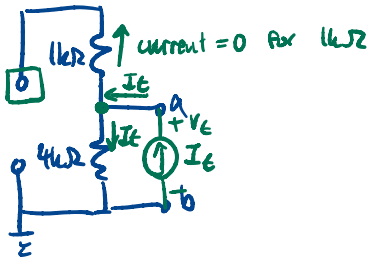
$I_N$

$I_N = I_{SC} = I_S = 5A$




(4kΩ resistor shorted out).

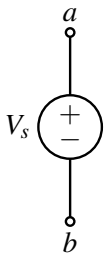
$R_{eq}$



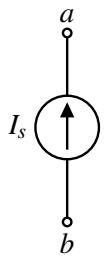

$V_t = 4k\Omega \cdot I_t$

$\frac{V_t}{I_t} = 4k\Omega = R_{eq} = R_{TH} = R_N$

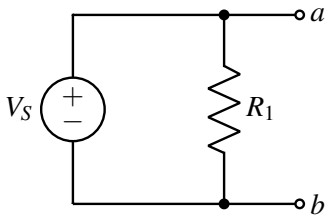
(c) **(Practice)**



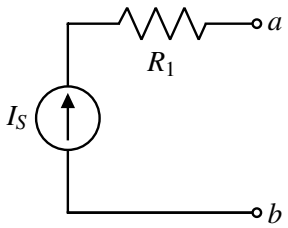
(d) **(Practice)**




(e) **(Practice)**




(f) **(Practice)**



**2. Finding Thévenin Equivalents**

(a) You are given the following $I_{out} - V_{out}$ characteristic of the Thévenin model of a circuit. Find the Thévenin voltage and the Thévenin resistance. Form a diagram in the style of Figure 1a (copied below for reference).

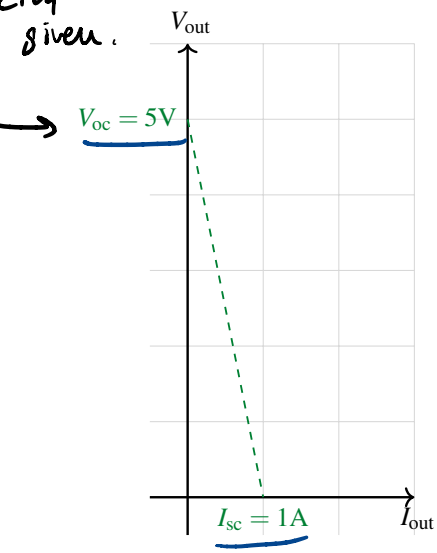
know $V_{TH}$ directly since $V_{OC}$ is given.

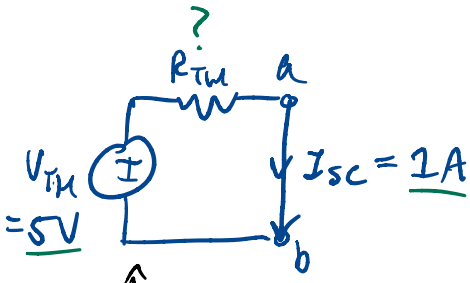
$V_{TH} = 5V$

$R_{eq} = \frac{V_{TH}}{I_N}$

$I_N = I_{SC} = 1A$

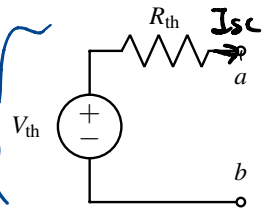
$R_{eq} = \frac{5V}{1A} = 5\Omega$



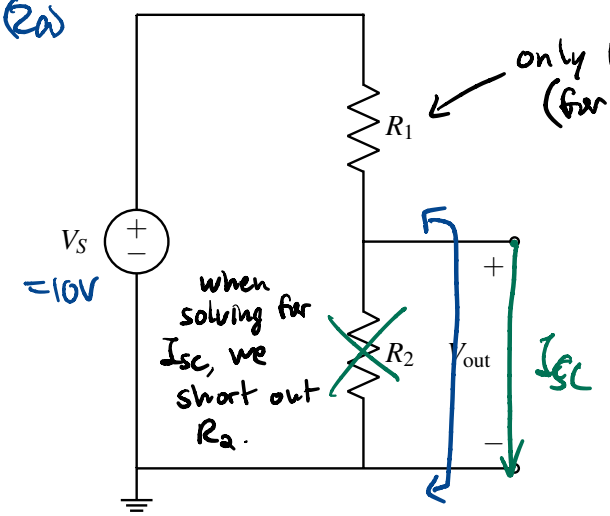

knowing $V_{TH} = 5V$ and $I_{SC} = 1A$, we find that $R_{eq} = 5\Omega$

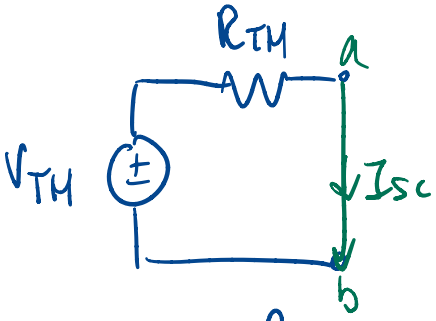
general thevenin model



(b) You are given a voltage divider as shown below. Find $R_1$ and $R_2$ such that the Thévenin equivalent model is the same as that of (a). You are given that $V_S = 10V$.

need: same Thevenin voltage
same equivalent resistance




$R_{eq} = R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$ } known from 1a)

$V_{TH} = V_S \cdot \frac{R_2}{R_1 + R_2}$

10V

$I_{sc} = 1A$

$V_{TH} = \frac{10 R_2}{R_1 + R_2} = 5V$

$\frac{1}{2} \Rightarrow R_1 = R_2$

but what specific value is it?

$R_{eq} = \frac{V_{TH}}{R_{TH}}$

$I_{sc} = \frac{V_S}{R_1}$

$1A = \frac{10V}{R_1}$

$\Rightarrow R_1 = 10\Omega$

$R_1 = R_2$
$\Rightarrow 10\Omega, 10\Omega$

Second method: (using $R_{eq}$ formula $R_1 \parallel R_2$ to find specific $R_1, R_2$ values)

since $R_1 = R_2$:
since $R_{eq} = R_1 \parallel R_2$ AND $R_{eq} = 5\Omega$
$\frac{R_1 R_2}{R_1 + R_2} = 5\Omega = \frac{R_1^2}{2R_1} \Rightarrow 10R_1 = R_1^2$
$\Rightarrow R_1 = 10\Omega$

### 3. NAND Circuit

Let us consider a NAND logic gate, as seen in Section 2. This circuit implements the boolean function $\overline{(A \cdot B)}$. The $\cdot$ stands for the AND operation, and the $\overline{\phantom{x}}$ stands for NOT; combining them, we get NAND!

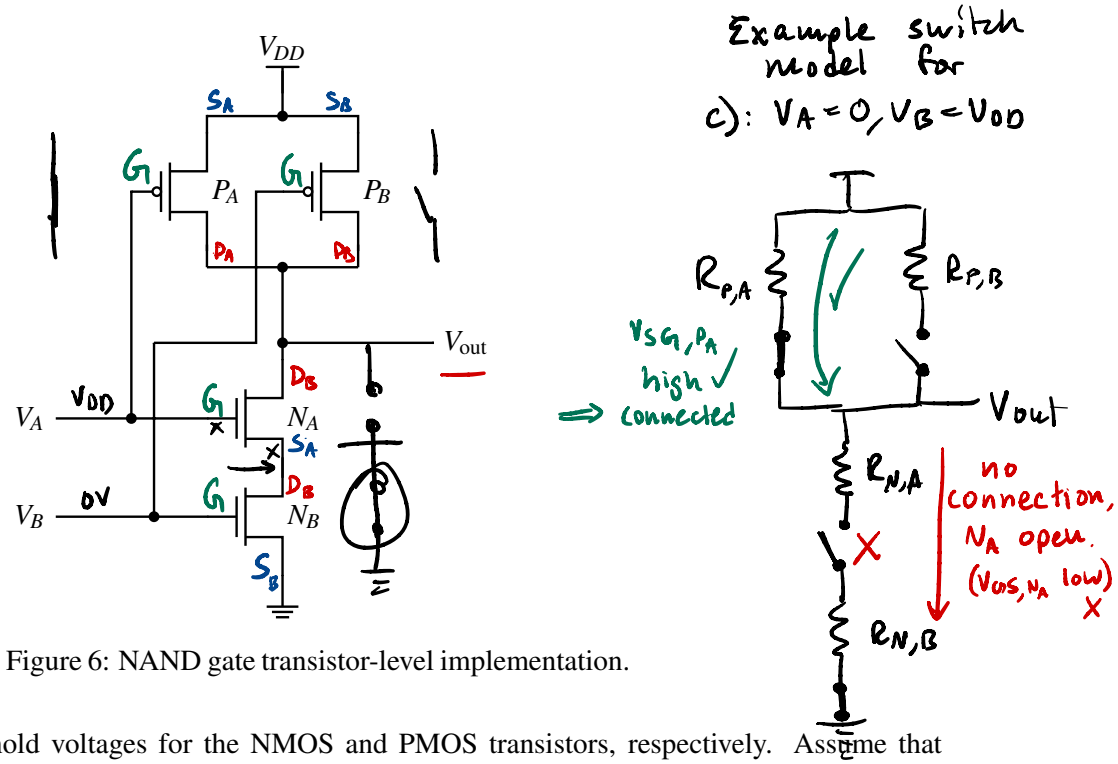



Figure 6: NAND gate transistor-level implementation.

$V_{tn}$ and $V_{tp}$ are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

(a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

(b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open switches? Which transistors act like closed switches? What is $V_{\text{out}}$?

$N_A, N_B$ are closed,
$P_A, P_B$ are open switches
$\Rightarrow V_{out} = 0V$

(c) If $V_A = 0V$ and $V_B = V_{DD}$, what is $V_{\text{out}}$?

$V_{out} = V_{DD}$
$P_B$ and $N_A$ are open
$P_A$ and $N_B$ are closed

(d) If $V_A = V_{DD}$ and $V_B = 0V$, what is $V_{\text{out}}$? → $P_A, N_B$ are open
$P_B, N_A$ are closed
$V_{out} = V_{DD}$

(e) If $V_A = 0V$ and $V_B = 0V$, what is $V_{\text{out}}$?

$V_{out} = V_{DD}$

$P_A, P_B$ both closed

$N_A, N_B$ both open

(f) Write out the truth table for this circuit.

| $V_A$ | $V_B$ | $V_{\text{out}}$ |
|---|---|---|
| 0 | 0 | $V_{DD}$ |
| 0 | $V_{DD}$ | $V_{DD}$ |
| $V_{DD}$ | 0 | $V_{DD}$ |
| $V_{DD}$ | $V_{DD}$ | 0 |

$\Rightarrow$ NAND!

(NOT AND)

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