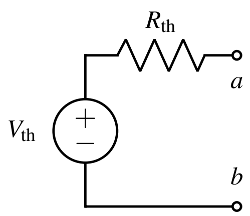
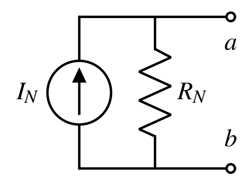
# EECS 16B Designing Information Devices and Systems II
# Spring 2021 Discussion Worksheet Discussion 2A

## 1 Circuit Equivalence

To review the circuit equivalence concepts exercised in this worksheet, please see Note 0B, adapted from the EECS 16A Course Notes. We will work through examples in this worksheet. The two forms are presented below for your reference.

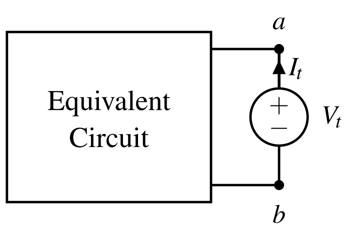



(a) General form of a Thévenin equivalent circuit. Given a circuit and two output terminals, we know the above gives a voltage-source based equivalent; the work lies in solving for $V_{th}$ and $R_{th}$.

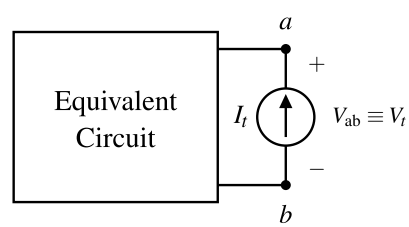



(b) General form of a Norton equivalent circuit, the current-source based equivalent form for a given circuit. Here, we must solve for $I_N$ and $R_N$.

Below, we display pictorially how to apply current or voltage test sources to a circuit to find $R_{eq}$.




(a) By applying a test voltage $V_t$ across $a$ and $b$, we can measure the resulting current draw of the equivalent circuit $I_t$ and use that to calculate $R_{eq}$.




(b) By feeding a test current $I_x$ into the equivalent circuit, we can measure the resulting voltage drop $V_{ab}$ and calculate $R_{eq}$.

Figure 2: We can use either a test voltage source or a test current source to find $R_{eq}$. The choice for what is easier will depend on the specific problem.

## 2 Transistor Introduction

Transistors (as presented in this course) are 3 terminal, voltage-controlled switches. This means that, when a transistor is "on," the Source (S) and Drain (D) terminals are connected via a low resistance path (short circuit). When a transistor is "off," the Source and Drain terminals are disconnected (open circuit).

Two common types of transistors are NMOS and PMOS transistors. Their states (shorted or open) are determined by comparing the voltage between the $G$ and $S$ terminals ($V_{GS} = V_G - V_S$) to a "threshold voltage"

($V_{tn}$ for NMOS, $V_{tp}$ for PMOS). Generally, NMOS transistors turn on when $V_{GS}$ is high enough, and PMOS transistors turn on when $V_{GS}$ is low enough (they have complementary behavior!). Transistors are extremely useful in digital logic design since we can use them to implement Boolean logic operators.

In this class, $V_{tn}$ denotes how much **higher** $V_G$ needs to be relative to $V_S$ for the NMOS to be on (allow current flow from drain to source), and $|V_{tp}|$ denotes how much **lower** $V_G$ gate needs to be relative to $V_S$ for the PMOS to be on.

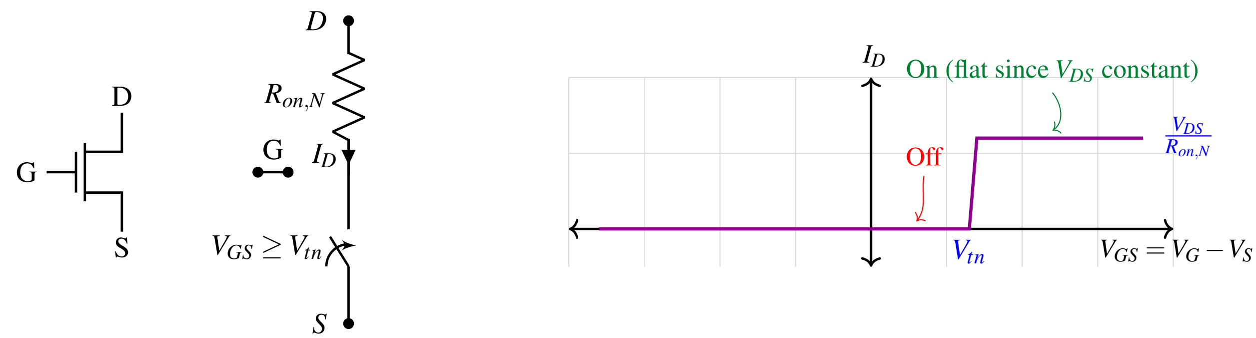



Figure 3: NMOS Transistor Resistor-switch model (the current holding constant at high $V_{GS}$ assumes that $V_{DS}$ is constant).

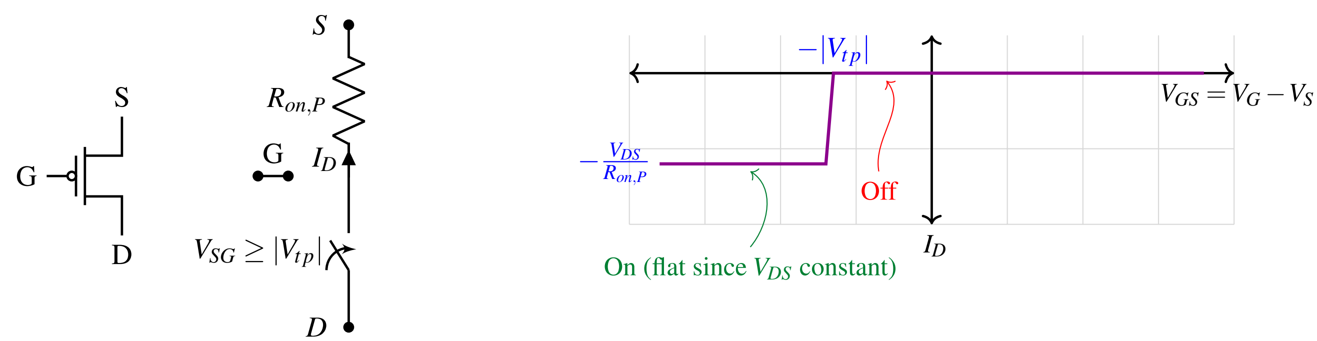



Figure 4: PMOS Transistor Resistor-switch model (the current holding constant at low $V_{GS}$ assumes that $V_{DS}$ is constant). Note that $V_{SG} = -V_{GS}$.

We mentioned that transistors can be connected to perform boolean algebra. An example of this is seen in Section 2, which is called an "inverter" and represents a NOT gate.

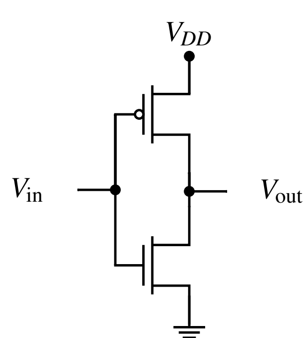



Figure 5: CMOS Inverter

To see why this circuit is called an inverter, we consider the following cases[1]:

(1) **The input is high**: $V_{\text{in}} = V_{DD}$. Then, since $V_{GS} \geq V_{tn}$ ($V_{\text{in}} \geq V_{tn}$), the NMOS is on. Also, since $V_{GS} \geq V_{tp}$ ($V_{\text{in}} - V_{DD} \geq V_{tp} \implies V_{\text{in}} \geq V_{DD} - |V_{tp}|$), the PMOS is off. So, only the NMOS switch is closed, and $V_{\text{out}} = 0$. That is, **the output is low**.

(2) **The input is low**: $V_{\text{in}} = 0$. Then, since $V_{GS} \leq V_{tn}$ ($V_{\text{in}} \leq V_{tn}$), the NMOS is off. Also, since $V_{GS} \leq V_{tp}$ ($V_{\text{in}} \leq V_{DD} - |V_{tp}|$), the PMOS is off. So, only the PMOS switch is closed, and $V_{\text{out}} = V_{DD}$. That is, **the output is high**.

We can summarize this analysis, using the following truth table:

| $V_{\text{in}}$ | $V_{\text{out}}$ | NMOS | PMOS |
|---|---|---|---|
| $V_{DD}$ | 0 | on | off |
| 0 | $V_{DD}$ | off | on |

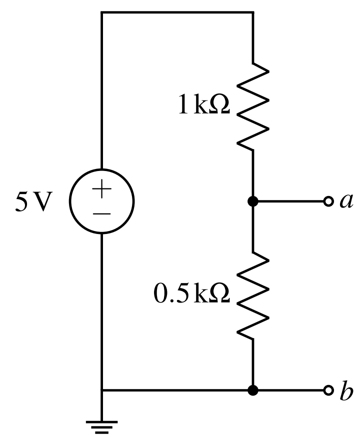
If you think of $V_{DD}$ being a logical 1 and 0V being a logical 0, we have just created the most elementary logical operation using transistors!

[1]When working with digital circuits like in Section 2, we usually only consider the values of $V_{\text{in}} = 0$ and $V_{\text{in}} = V_{DD}$.

**1. Thévenin and Norton Equivalence**

Find the Thévenin and Norton equivalents across terminals $a$ and $b$ for the circuits given below. Note that the general forms of these equivalents can be found in Figure 1a and Figure 1b.

(a)



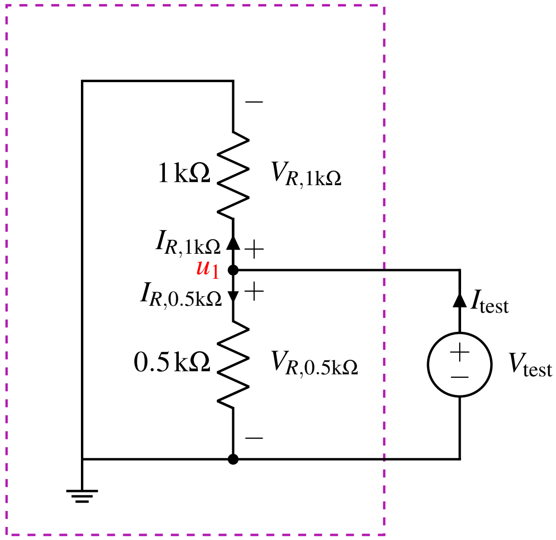

**Answer:** We can apply the definition of the Thévenin and Norton equivalents to solve this problem by first finding the open-circuit voltage and the short-circuit current. Since the terminals $a$ and $b$ are already disconnected (open), finding $V_{\text{th}}$ is the same as finding the voltage drop across the bottom 0.5kΩ resistor. Applying the voltage divider formula, this is:

$$V_{\text{th}} = 5 \cdot \frac{0.5\text{k}\Omega}{1\text{k}\Omega + 0.5\text{k}\Omega} = 1.67\text{V}$$

To find the short-circuit current ($I_N$), we connect terminals $a$ and $b$ with a wire and find the resulting current flow through that wire, between the terminals. Attaching such a wire shorts out the 0.5kΩ resistor, so all that remains is the top 1kΩ resistor. The current that flows is $\frac{V_S}{R_{\text{eq}}}$. That is:

$$I_N = \frac{5\text{V}}{1\text{k}\Omega} = 5\text{mA}$$

Finally, to find the equivalent resistance between the terminals, we have 3 options. We will present the $\frac{V_{\text{test}}}{I_{\text{test}}}$ option discussed in the associated lecture, and leave the other options as Alternate Solutions below. We first form a test-circuit as in Figure 2a. Then, we zero out the independent sources (here, the 5V voltage source.) Recall that a zeroed voltage source becomes a wire (which has zero voltage across it, by definition). So, our circuit diagram looks as follows:




Now, we perform nodal analysis; at the node labeled $u_1$, we write:

$$I_{\text{test}} = I_{R,1\text{k}\Omega} + I_{R,0.5\text{k}\Omega}$$

This then becomes (after substituting in Ohm's Law equations):

$$\begin{aligned} I_{\text{test}} &= \frac{V_{R,1\text{k}\Omega}}{1\text{k}\Omega} + \frac{V_{R,0.5\text{k}\Omega}}{0.5\text{k}\Omega} \\ &= \frac{V_{\text{test}}}{1\text{k}\Omega} + \frac{V_{\text{test}}}{0.5\text{k}\Omega} \end{aligned}$$

Solving the algebra, we find that $\frac{V_{\text{test}}}{I_{\text{test}}} = R_{\text{th}} = 333\Omega$.

**Alternate Solutions to Find $\mathbf{R_{th}}$**: Another option is to use the calculated values of $V_{\text{th}}$ and $I_N$ to find that $R_{\text{eq}} = \frac{V_{\text{th}}}{I_N} = 333\Omega$. This might be more convenient given that we already solved for $V_{\text{th}}$ and $I_N$ but the systematic approach is important to know. We can also illustrate one last technique for completeness by using resistor network simplifications after explicitly zeroing all independent sources to calculate $R_{\text{eq}}$ (which we can do since there are no dependent sources in the circuit).

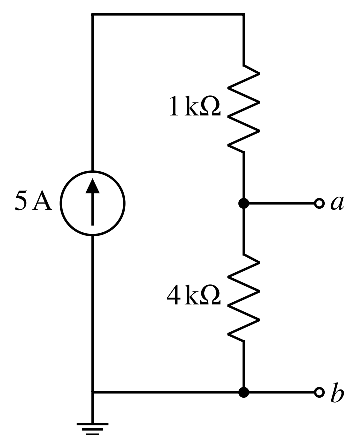
To approach the problem in this way, the primary insight required is to note that from the perspective of terminals $a$ and $b$, the resistors are actually in *parallel*. This is because the voltage source becomes a short when zeroed out following the procedure, and the two resistors actually now share the same terminal nodes (the 0.5kΩ resistor has terminal $a$ on top and $b$ on the bottom, whereas the 1kΩ resistor has terminal $a$ on the bottom and, through the shorted voltage source, terminal $b$ on the top.) Therefore, the equivalent resistance seen by $a$ and $b$ is:

$$R_{\text{eq}} = (0.5 \parallel 1)\text{k}\Omega = 333\Omega$$

See Figure 6 for labeled versions of the equivalent circuits.


Figure 6: Answers for part a).

(b)



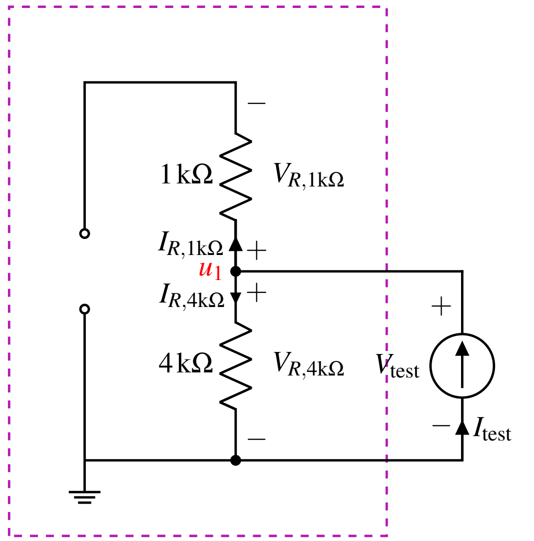

**Answer:** We can once again apply the definitions as in part a).
*Open-circuit voltage*: The terminals $a$ and $b$ are already disconnected (open), so we find $V_{\text{th}} = V_{4\text{k}\Omega}$. Noting that we have a current source in this circuit, we apply Ohm's Law to find:

$$V_{\text{th}} = I_S \cdot R = 5\text{A} \cdot 4\text{k}\Omega = 20\text{kV}$$

*Short-circuit current*: We short terminals $a$ and $b$ and find the resulting current flow. Since we have a current source and all of that current will go through the short (none will go through the 4kΩ resistor), we find that:

$$I_N = 5\text{A}$$

To find the equivalent resistance, we can feed in a test current source, as seen below. Doing so, we find that since the top branch is an open-circuit (a zeroed current-source is an open circuit), no current can flow in that path. Therefore, all of the $I_{\text{test}}$ current will flow through the 4kΩ resistor, generating a voltage drop of $V_{\text{test}} = I_{\text{test}} \cdot 4\text{k}\Omega$. We then find directly that $\frac{V_{\text{test}}}{I_{\text{test}}} = R_{\text{eq}} = 4\text{k}\Omega$.



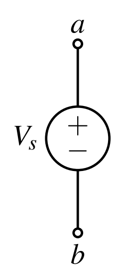

**Alternate Solutions to Find $\mathbf{R_{th}}$**: We can now use $V_{\text{th}}$ and $I_N$ to find that $R_{\text{eq}} = \frac{V_{\text{th}}}{I_N} = 4\text{k}\Omega$, or we can repeat the process above (zero out independent sources and calculate $R_{\text{eq}}$ explicitly). Note that here, the independent source we zero out is a current source, which becomes an open circuit. Therefore, there is only one path between $a$ and $b$ through the $4\text{k}\Omega$ resistor, and the equivalent resistance seen is:

$$R_{\text{eq}} = 4\text{k}\Omega$$

See Figure 7 for labeled versions of the equivalent circuits.

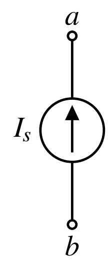

Figure 7: Answers for part b).

(c) **(Practice)**



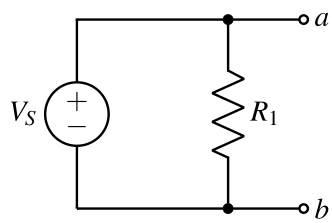

**Answer:** This subpart tests one's conceptual understanding of circuit equivalences. Here, we are given a voltage source, which is its own Thévenin equivalent (in Figure 1a, $R_{\text{th}} = 0$). It also does not make sense to form a Norton equivalent here! If we short the two terminals of a voltage source, a very large amount of current can flow, so without any series resistance, a Norton equivalent cannot be formed. We say that since a voltage source is a "basic circuit element", we cannot represent it with a current source model.

(d) **(Practice)**




**Answer:** A current source is its own Norton equivalent (in Figure 1b, $R_{\text{th}} = \infty$ since no current flows in the source's own parallel resistance). As in part c), it does not make sense to form a Thévenin equivalent here, since a current source is a "basic element" and cannot be represented with a voltage source model.

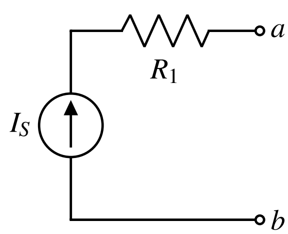
(e) **(Practice)**




**Answer:** The Thévenin equivalent is just a voltage source with voltage $V_S$, that is, $R_{\text{th}} = 0$. Notice that adding a parallel resistor does not change the Thévenin equivalent, since the voltage source will always maintain $V_S$ volts across its terminals. Note that this potential difference holds even if we add a circuit component between terminals $a$ and $b$. However, when the resistance is in *series* with the voltage source, adding a circuit element between $a$ and $b$ causes current to flow in the loop, and there is subsequently a voltage division from the source to the output.

As before, since the circuit is effectively a voltage source, it does not make sense to form a Norton equivalent.

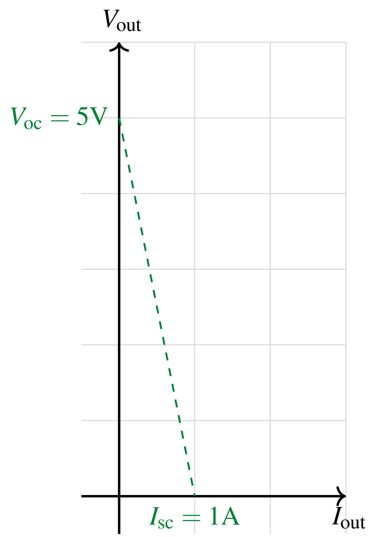
(f) **(Practice)**

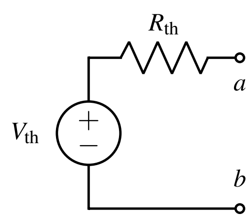



**Answer:** The Norton equivalent is just a current source with current $I_S$, that is, $R_N = \infty$. Adding a series resistor does not change the Norton equivalent because when $a$ and $b$ are shorted, the current source will always supply $I_S$ amps. With a similar argument as before, it does not make sense to form a Thévenin equivalent for this circuit, as it functions as a basic circuit element.

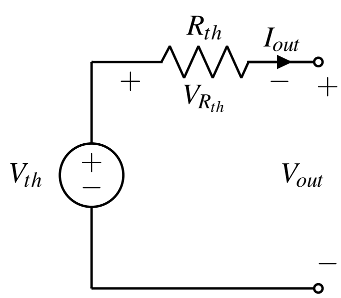
## 2. Finding Thévenin Equivalents

(a) You are given the following $I_{\text{out}} - V_{\text{out}}$ characteristic of the Thévenin model of a circuit. Find the Thévenin voltage and the Thévenin resistance. Form a diagram in the style of Figure 1a (copied below for reference).

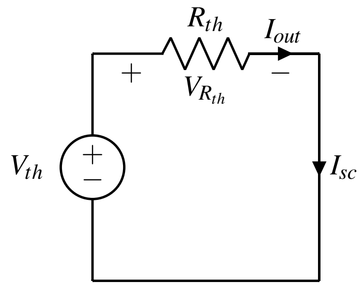



**Answer:** The Thévenin voltage is the open circuit voltage of the circuit. From the $I_{\text{out}} - V_{\text{out}}$ characteristic, we see that this is 5V here. Observing the diagram and invoking KVL reveals that $V_{\text{th}} + V_{R_{\text{th}}} + V_{\text{out}} = 0$. Additionally, $I_{\text{out}} = I_{R_{\text{th}}}$ by KCL.



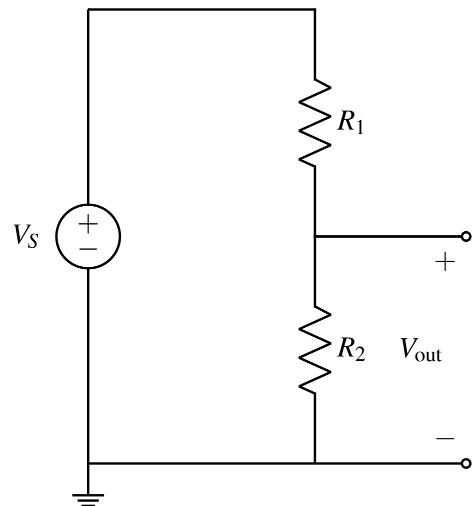

When the output is shorted, $I_{\text{out}} = I_{\text{sc}}$, and $V_{out} = 0\text{V}$ (no voltage drop across a wire), which implies that $V_{R_{\text{th}}} = V_{\text{th}}$, and $I_{R_{\text{th}}} = I_{\text{sc}}$.




Thus by Ohm's law, the Thévenin resistance is equal to $R_{th} = \frac{V_{R_{\text{th}}}}{I_{R_{\text{th}}}} = \frac{V_{\text{th}}}{I_{\text{sc}}}$. That is:

$$R_{\text{th}} = 5\Omega$$

(b) You are given a voltage divider as shown below. Find $R_1$ and $R_2$ such that the Thévenin equivalent model is the same as that of (a). You are given that $V_S = 10V$.




**Answer:** From part (a), $V_{\text{th}} = 5\text{V}$.
Earlier in this worksheet, we solved for the Thévenin voltage $V_{\text{th}}$ of the voltage divider, which is equal to $V_{\text{th}} = V_S \frac{R_2}{R_1+R_2}$. Here, we need to set the two expressions equal; the value of the Thévenin voltage we want, and the symbolic expression for the voltage divider's Thévenin voltage. Equating and solving:

$$\begin{aligned} 5\text{V} &= 10\text{V}\frac{R_2}{R_1+R_2} \\ 5R_1 + 5R_2 &= 10R_2 \\ 5R_2 &= 5R_1 \end{aligned}$$

Therefore $R_1 = R_2$. But this doesn't yet give us the specific values. To find that, we bring in the next requirement we have, which is that $I_{\text{sc}} = 1\text{A}$. If we short the output of the voltage divider, then as we saw previously (since $R_2$ becomes shorted out), we have:

$$I_{\text{sc}} = \frac{V_S}{R_1} = \frac{10}{R_1} = 1\text{A}$$

Therefore $R_1 = 10\Omega$ and $R_2 = 10\Omega$.

**3. NAND Circuit**

Let us consider a NAND logic gate, as seen in Section 2. This circuit implements the boolean function $\overline{(A \cdot B)}$. The $\cdot$ stands for the AND operation, and the $\overline{\quad}$ stands for NOT; combining them, we get NAND!

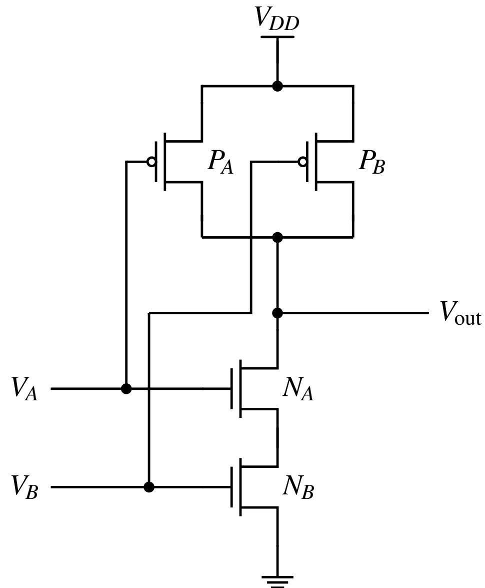



Figure 8: NAND gate transistor-level implementation.

$V_{tn}$ and $V_{tp}$ are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

(a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

**Answer:** In an NMOS, the terminal at the higher potential is always the drain, and the terminal at the lower potential is always the source. Therefore, the drains are at the top of $N_A$ (connected to $V_{\text{out}}$) and the top of $N_B$ (connected to $N_A$). The sources are at the bottom of $N_A$ (connected to $N_B$) and the bottom of $N_B$ (connected to ground). The gate terminal of $N_A$ is connected to $V_A$; the gate of $N_B$ is connected to $V_B$.

In a PMOS, the terminal at the higher potential is always the source, and the terminal at the lower potential is always the drain. Therefore, the source is at the top of $P_A$ and $P_B$ (connected to $V_{DD}$). The drain is at the bottom of $P_A$ and $P_B$ (connected to $V_{\text{out}}$). The gate terminal of $P_A$ is connected to $V_A$; the gate of $P_B$ is connected to $V_B$.

(b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open switches? Which transistors act like closed switches? What is $V_{\text{out}}$?

**Answer:** $P_A$ and $P_B$ are off (open switches). $N_B$ and $N_A$ are on (closed switches). $V_{\text{out}} = 0\text{V}$ because it is connected to ground through a closed circuit consisting of $P_A$ and $P_B$ (and detached from $V_{DD}$).

(c) If $V_A = 0V$ and $V_B = V_{DD}$, what is $V_{\text{out}}$?

**Answer:** $P_B$ and $N_A$ are off (open switches). $P_A$ and $N_B$ are on (closed switches). $V_{\text{out}} = V_{DD}$ because it is connected to $V_{DD}$ through a closed circuit consisting of $P_A$ (and detached from ground, since *both* $N_A$ and $N_B$ must be closed for $V_{\text{out}}$ to be connected to ground).

(d) If $V_A = V_{DD}$ and $V_B = 0V$, what is $V_{\text{out}}$?

**Answer:** $P_A$ and $N_B$ are off (open switches). $P_B$ and $N_A$ are on (closed switches). But, since $N_B$ is open, $N_A$ being closed doesn't connect $V_{\text{out}}$ to ground. So, $V_{\text{out}} = V_{DD}$ because it is connected to $V_{DD}$ through a closed switch.

Note that with the simplest transistor model, one cannot to determine $V_{GS}$ for $N_A$, since we don't know the source voltage for that transistor. $V_{\text{out}}$ is still high, because regardless of whether $N_A$ is on, there is an open (or very high resistance) between $V_{\text{out}}$ and ground while there is a short to $V_{DD}$.

(e) If $V_A = 0V$ and $V_B = 0V$, what is $V_{\text{out}}$?

**Answer:** $N_B$ is off, creating an open circuit. $P_A$ and $P_B$ are on, creating a closed circuit. $V_{\text{out}} = V_{DD}$ because it is connected by closed circuit to $V_{DD}$.

Like above, the source of $N_A$ has an ambigous value and we cannot determine whether $N_A$ is on or off. However, this doesn't affect the output because the path to ground is an open (since $N_B$ is definitely off, $V_{GS,N_A} = 0 \leq V_{tn}$.

(f) Write out the truth table for this circuit.

| $V_A$ | $V_B$ | $V_{\text{out}}$ |
|---|---|---|
| 0 | 0 | |
| 0 | $V_{DD}$ | |
| $V_{DD}$ | 0 | |
| $V_{DD}$ | $V_{DD}$ | |

**Answer:**

| $V_A$ | $V_B$ | $V_{\text{out}}$ |
|---|---|---|
| 0 | 0 | $V_{DD}$ |
| 0 | $V_{DD}$ | $V_{DD}$ |
| $V_{DD}$ | 0 | $V_{DD}$ |
| $V_{DD}$ | $V_{DD}$ | 0 |

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