1 First-Order Differential Equation Practice

a) Solve the equation $\frac{d}{dt}f(t) = 2f(t)$ given that $f(0) = 5$.

Solution

The solution to a homogeneous first-order differential equation

$$\frac{d}{dt}x(t) = \lambda x(t)$$

is of the form $x(t) = Ae^{\lambda t}$. Therefore, the solution to this differential equation will be of the form $f(t) = Ae^{2t}$. Plugging in the initial condition, we see that

$$f(0) = Ae^0 = A = 5$$

Therefore, we conclude that the solution to the differential equation is $f(t) = 5e^{2t}$.

b) Solve the equation $3\frac{d}{dt}f(t) + 6f(t) = 0$ given that $f(0) = 7$.

Solution

We can rewrite this differential equation in the following form:

$$\frac{d}{dt}f(t) = -2f(t)$$

Recall from the previous part that this differential equation has a solution of the form $f(t) = Ae^{-2t}$. To solve for A, we plug in the initial condition and see that

$$f(0) = Ae^0 = A = 7$$

Therefore, the solution to the differential equation is $f(t) = 7e^{-2t}$.

c) Solve the equation $3f(t) - 6\frac{d}{dt}f(t) = 4$ given that $f(2) = \frac{1}{3}$.

Solution

This is a first-order non-homogeneous differential with a constant term. Since $\lambda = \frac{1}{2}$, the solution will be of the form $f(t) = Ae^{\frac{1}{2}t} + B$. Plugging in our guess into the differential equation, we see that

$$3(Ae^{\frac{1}{2}t} + B) - 6(\frac{1}{2}Ae^{\frac{1}{2}t}) = 4$$
$$(3A - 3A)e^{\frac{1}{2}t} + 3B = 4$$

This tells us that $B = \frac{4}{3}$. Lastly, to solve for A we plug in the initial condition

$$f(2) = Ae + \frac{4}{3} = \frac{1}{3}$$
$$\implies A = -e^{-1}$$

Therefore, the solution to this differential equation is $f(t) = -e^{\frac{1}{2}t-1} + \frac{4}{3}$.

d) Solve the equation $f(t) - a\frac{d}{dt}f(t) = b$, given that $f(t_0) = b$ and $a \neq 0$.

Solution

This is a first-order non-homogeneous differential with a constant term. Since $\lambda = \frac{1}{a}$, the solution will be of the form $f(t) = Ae^{t/a} + B$.

$$\begin{aligned} f(t) - a\frac{d}{dt}f(t) &= b \\ (Ae^{t/a} + B) - a(\frac{1}{a}Ae^{t/a}) &= b \\ \implies B &= b \end{aligned}$$

To solve for A we plug in the initial condition

$$\begin{aligned} f(t_0) &= Ae^{t_0/a} + b = b \\ \implies Ae^{t_0/a} &= 0 \end{aligned}$$

The quantity $e^{t_0/a} > 0$ for any value of t_0 so A must be equal to 0. Thus the solution to the differential equation is $f(t) = b$.

Note: Our solution $f(t)$ is a constant without an exponential term. Let's try to break down why this is the case. First consider the differential equation of the form

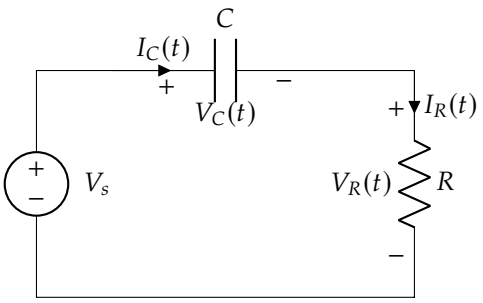
$$\frac{d}{dt}x(t) = \lambda x(t); \quad x(0) = 0$$

You'll notice that the solution is $x(t) = 0$.

In our case, the solution $f(t) = Ae^{\lambda t} + B$. The $Ae^{\lambda t}$ term represents some change that $f(t)$ will make from its initial state whereas B represents the final state given $\lambda < 0$.

Since we showed that the steady state of $f(t)$ is b, and our initial condition $f(t_0) = b$, the function f doesn't need to move at all to reach b. It's already at b.

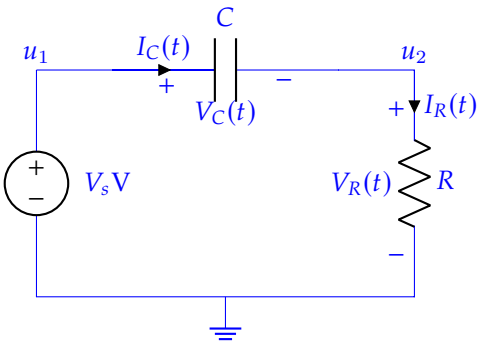
2 RC Circuit



a) Find a differential equation for $V_c(t)$ for $t \geq 0$. Solve the differential equation using the initial condition $V_c(0) = 1\text{V}$. Use component values of $C = 1\text{fF}$ ($1\text{fF} = 10^{-15}\text{F}$), $R = 10\text{k}\Omega$, and $V_s = 2\text{V}$

Solution

First, we set one node to ground and label the other two nodes as u_1 and u_2.



$$
\begin{aligned}
V_c(t) &= u_1 - u_2 \\
u_1 &= V_s \\
u_2 &= V_R(t) \\
V_c(t) &= V_s - V_R(t)
\end{aligned} \tag{1}
$$

Using Ohm's law:

$$V_R(t) = RI_R(t)$$

Using KCL at u_2

$$
\begin{aligned}
I_R(t) &= I_C(t) \\
V_R(t) &= RI_C(t)
\end{aligned}
$$

The current through a capacitor is:

$$I_C(t) = C\frac{dV_C(t)}{dt}$$
$$V_R(t) = RC\frac{dV_C(t)}{dt}$$

Plugging back into (1):

$$V_c(t) = V_s - RC\frac{dV_C(t)}{dt}$$

Rearranging, we get our differential equation:

$$\frac{dV_C(t)}{dt} + \frac{V_C(t)}{RC} = \frac{V_s}{RC}$$

This is a first-order non-homogeneous differential equation that can be solved through Guess and Check of Substitution of Variables.

$$V_C(t) = 2 - e^{-\frac{t}{10^{-11}}} \text{ [V]}$$

b) Instead of having an initial condition of $V_c(0) = 1$V, we now have an initial condition of $I_R(0) = 150\mu$A (1μA $= 10^{-6}$A). Find the new expression for $V_C(t)$ for $t \geq 0$. Use the same component values listed in part (a)

Solution

We can use the same general solution as in part (a), but we need to plug in our new initial condition to solve for A. To do that, we need to determine what $V_C(0)$ is using our current's initial condition.

Using Ohm's law:

$$V_R(0) = I_R(0) * R = 150 * 10^{-6} * 10^4 = 1.5 \text{ V}$$

We know that:

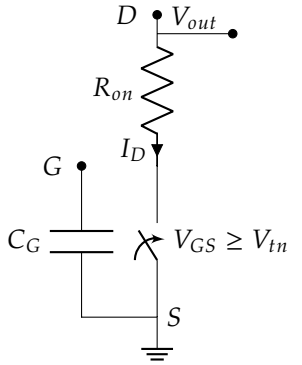
$$V_C(0) = V_s - V_R(0) = 2 - 1.5 = 0.5 \text{ V}$$

Now we can plug it back into the general solution to get:

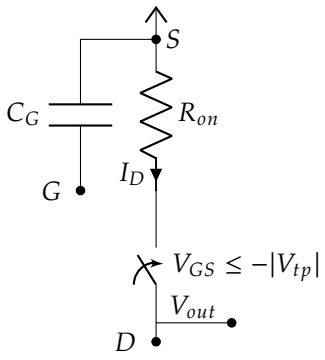
$$V_C(t) = 2 - 1.5e^{-\frac{t}{10^{-11}}} \text{ [V]}$$

3 Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitance C_G represents the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model



(b) PMOS Transistor Resistor-switch-capacitor model.

Figure 1: Note: We have drawn this so that it aligns with the inverter shown below.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_G = 1\text{fF}$ (femto-Farads = 10^{-15}). The supply voltage V_{DD} is 1Vand the two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (fig. 2).

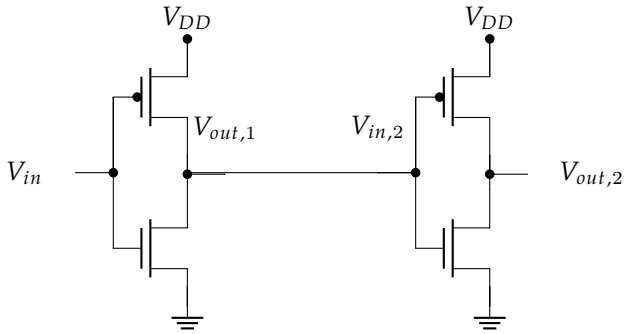


Figure 2: CMOS Inverter chain

a) Assume the input to the first inverter has been low ($V_{in} = 0\ \text{V}$) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,1}$) for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

Solution

Before $t = 0$, the input to the first inverter was low for a long time. This means that for $t < 0$, the output of the inverter ($V_{out,1}$) had been held at V_{DD} for a long time.

At $t = 0$, the input goes high. This means the input inverter's NMOS device turns on connecting $V_{out,1}$ to ground through a resistance of R_{on}. The inverter's PMOS device is off meaning we have an open circuit from V_{DD} to V_{out}.

At the input node, V_{in}, no current flows through the two gate capacitors ($I_p = I_n = 0$.) This is because the current is proportional to the change in voltage across the capacitors. However, the voltage difference across the top capacitor stays at 0 and the difference across the bottom capacitor stays at V_{DD}.

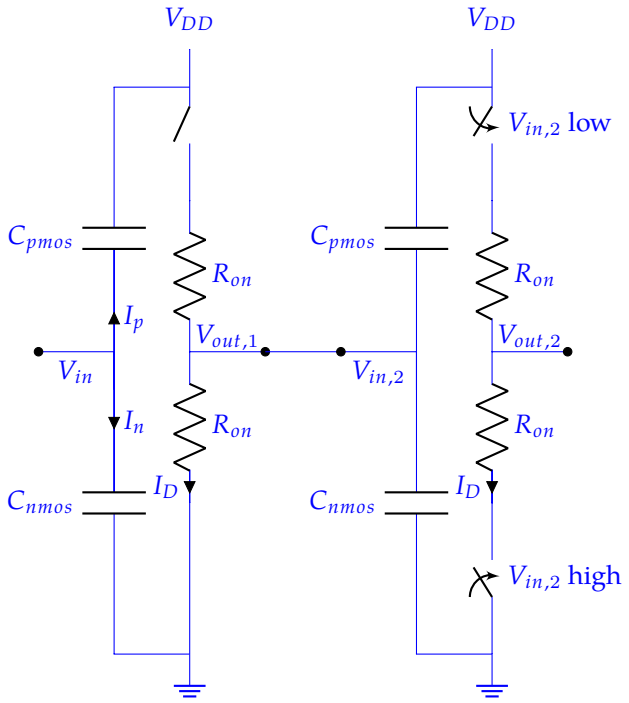


Figure 3: $V_{in} = V_{DD}$ so the PMOS is off and the NMOS is on.

The second inverter "loads" the output of the first inverter. From the notes in the problem, we can model the gates of the transistors as capacitors. These gates together form our capacitive load. The gate of the pmos acts as a capacitor to V_{DD} and the gate of the nmos acts as a capacitor to ground. Using this we can draw the following RC circuit:

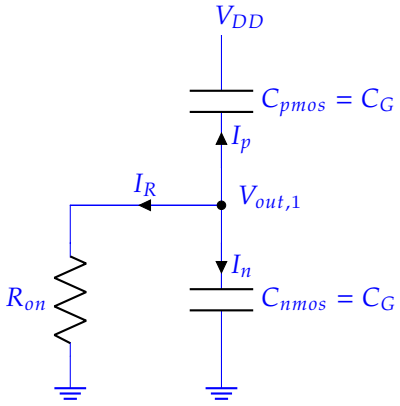


Figure 4: First inverter output at 0

We know the voltage across C_{pmos} is $V_{out,1}(t) - V_{DD}$ and the voltage across C_{nmos} is $V_{out,1}(t)$. Using this information, we can set up a KCL equation and use the i-v relationship of a capacitor:

$$I_p = C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \qquad I_n = C_{nmos}\frac{d}{dt}V_{out,1}(t)$$
$$I_R = \frac{V_{out,1}(t)}{R_{on}} \qquad I_p + I_n + I_R = 0$$

Then we can set up a differential equation to solve for $V_{out}(t)$:

$$C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{nmos}\frac{d}{dt}V_{out,1}(t) + \frac{V_{out,1}(t)}{R_{on}} = 0$$
$$C_{pmos}\frac{d}{dt}V_{out,1}(t) + C_{nmos}\frac{d}{dt}V_{out,1}(t) + \frac{V_{out,1}(t)}{R_{on}} = 0$$
$$(C_{pmos} + C_{nmos})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}}$$
$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{R_{on}(C_{pmos} + C_{nmos})}$$
$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t)}{2R_{on}C_G}$$

b) Given the initial conditions in part (a), **solve for** $V_{out,1}(t)$**.**

Solution

We know that the solution to a differential equation of the form

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}}{R_{on}(2C_G)}$$

is

$$V_{out,1}(t) = ke^{-\frac{t}{R_{on}(2C_G)}}$$

Plugging in the initial condition $V_{out,1}(0) = V_{DD}$ we find that $V_{out,1}(t) = V_{DD}e^{-\frac{t}{R_{on}(2C_G)}}$.

c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

Solution

(1) We know that the output of our inverter started with the initial value V_{DD}.

(2) Since the differential equation tells us the change in value of $V_{out,1}(t)$ at time t we can simply plug in $t = 0$ into our differential equation to get the initial slope:

$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(0)}{R_{on}(C_{nmos} + C_{pmos})} \tag{1}$$

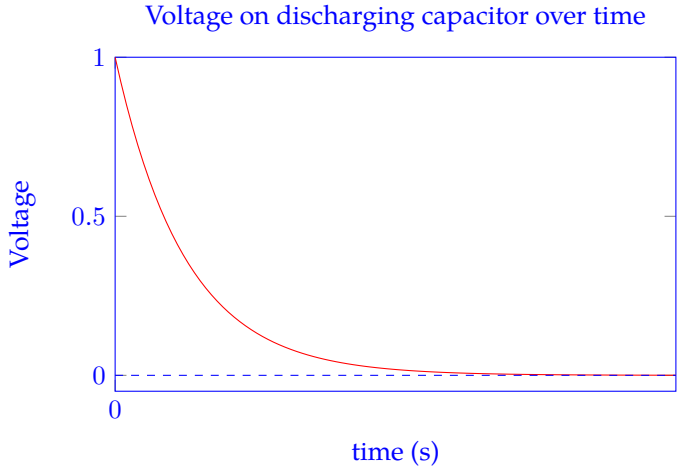
$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{DD}}{R_{on}(C_{nmos} + C_{pmos})} \tag{2}$$

Thus the initial slope is $-\frac{V_{DD}}{R_{on}(C_{nmos}+C_{pmos})} = -\frac{V_{DD}}{R_{on}(2C_G)}$

(3) Since the input to the inverter changed from low to high we know the output of the first inverter ($V_{out,1}$) is going to go to 0 in steady state, as this node will be discharged by the first inverter's nmos transistor.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD}e^{-\frac{\infty}{R_{on}(2C_G)}} = 0$.

(4) To approximate when the output will decay to $\frac{1}{3}$ its original value, we use the fact that $e^{-1} = \frac{1}{e} \approx \frac{1}{3}$. We thus want to find when $V_{out,1} = V_{DD}e^{-1}$. This will occur when the e term is raised to -1, which occurs when $t = R_{on}(2C_G) = 2 \times 10^{-12}$ s.



d) A long time later, the input to the first inverter switches low again. **Solve for $V_{out,1}(t)$.**

Solution

We know that after a long time, the output of the first inverter has stabilized to 0. When the input switches low again, the input inverter's nmos device turns off, while the input inverter's pmos device turns on. This connects the $V_{out,1}$ node to V_{DD}, as shown in fig. 7.

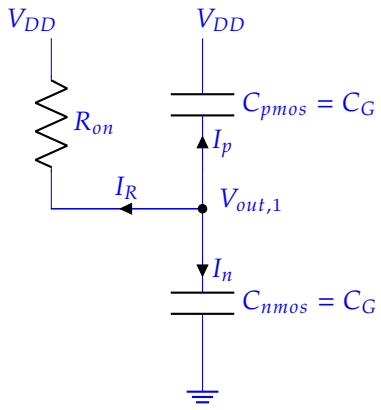


Figure 5: Inverter output at 1

To set up the differential equation, we apply KVL and KCL again:

$$I_p = C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) \qquad I_n = C_{nmos}\frac{d}{dt}V_{out,1}(t)$$
$$I_R = \frac{V_{out,1}(t) - V_{DD}}{R_{on}} \qquad I_p + I_n + I_R = 0$$

Then we can set up a differential equation to solve for $V_{out}(t)$:

$$C_{pmos}\frac{d}{dt}(V_{out,1}(t) - V_{DD}) + C_{nmos}\frac{d}{dt}V_{out,1}(t) + \frac{V_{out,1}(t) - V_{DD}}{R_{on}} = 0$$
$$C_{pmos}\frac{d}{dt}V_{out,1}(t) + C_{nmos}\frac{d}{dt}V_{out,1}(t) + \frac{V_{out,1}(t) - V_{DD}}{R_{on}} = 0$$
$$(C_{pmos} + C_{nmos})\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}}$$
$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{R_{on}(C_{pmos} + C_{nmos})}$$
$$\frac{d}{dt}V_{out,1}(t) = -\frac{V_{out,1}(t) - V_{DD}}{2R_{on}C_G}$$

We know that a differential equation of the form $\frac{d}{dt}x(t) + \alpha x(t) = \beta$ has solution

$$x(t) = x_0 e^{-\alpha t} + \frac{\beta}{\alpha}(1 - e^{-\alpha t})$$

Substituting for $x(t) = V_{out,1}, x_0 = 0, \alpha = \frac{1}{2R_{on}C_G}, \beta = \frac{V_{DD}}{2R_{on}C_G}$, we get:

$$V_{out,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{2R_{on}C_G}}\right)$$

e) **Sketch the output voltage of the first inverter ($V_{out,1}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.**

Solution

(1) Because the input to the first inverter was high for a long time, we know the initial value of $V_{out,1}(t) = 0$. This was the initial condition applied to the solution of the differential equation, above.

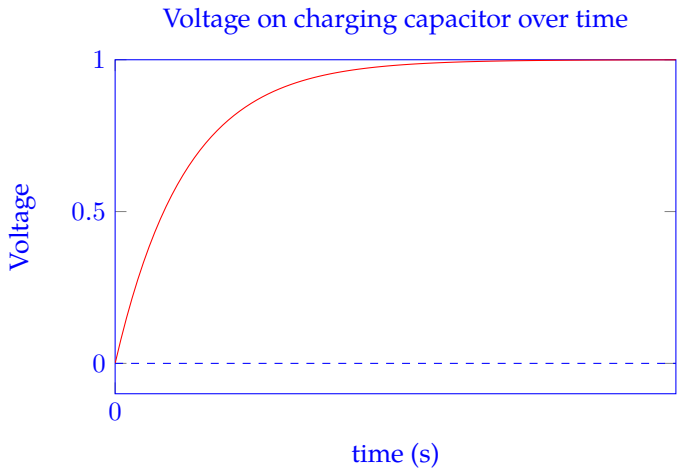
(2) To find the initial value of the slope we can plug in $t = 0$ to the above differential equation:

$$\frac{d}{dt}V_{out,1}(t = 0) = \frac{(V_{DD} - V_{out,1}(0))}{R_{on}(2C_G)}$$

where $V_{out,1}(0) = 0$. Thus our initial slope is $\frac{(V_{DD})}{R_{on}(2C_G)}$. Notice this slope is positive while the previous part had a negative slope.

(3) Since the input to the inverter changed from high to low and the input inverter's pmos is now on, we know the output of the first inverter is going to go to V_{DD} in steady state.

Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{out,1}(t)$ to find $V_{out,1} = V_{DD}\left(1 - e^{-\frac{\infty}{R_{on}(2C_G)}}\right) = V_{DD}(1 - 0) = V_{DD}$.



f) For each complete input cycle described above ($V_{in} = 0\text{V} \rightarrow 1\text{V} \rightarrow 0\text{V}$), **how much charge is pulled out of the power supply?** Give both a symbolic and numerical answer. **Consider only the charge needed to charge up the $V_{out,1}$ node.**

Solution

To find the charge required from the supply, we can integrate the current required from the supply during each phase of the cycle ($Q = \int_0^\infty I_{V_{DD}}(t)dt$).
The ciruit in the input step, $0 \rightarrow 1$ is drawn below. We know that the voltage is $V_{out,1}(t) = V_{DD}e^{-\frac{t}{2C_G R_{on}}}$.

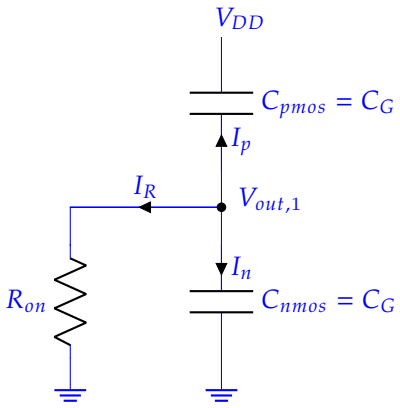


Figure 6: Process $0 \rightarrow 1$

Here only the current I_p affects the amount of charge pulled out of V_{DD}.

$$\begin{aligned} I_p(t) &= C_G \frac{d}{dt}(V_{out,1}(t) - V_{DD}) \\ &= C_G \frac{-1}{2C_G R_{on}} V_{DD} e^{-\frac{t}{2C_G R_{on}}} \end{aligned}$$

Thus:

$$\begin{aligned} Q_{0\rightarrow 1} &= \int_0^\infty I_{C_{pmos}}(t)dt = \int_0^\infty C_G \frac{-1}{2C_G R_{on}} V_{DD} e^{-\frac{t}{2C_G R_{on}}} dt \\ &= C_G \cdot V_{DD} e^{-\frac{t}{2C_G R_{on}}} |_0^\infty \\ &= C_G \cdot V_{DD}(0-1) = -C_G \cdot V_{DD} \end{aligned}$$

The ciruit in the input step, $0 \rightarrow 1$ is drawn below. We know that the voltage is $V_{out,1}(t) = V_{DD}\left(1 - e^{-\frac{t}{2R_{on}C_G}}\right)$.

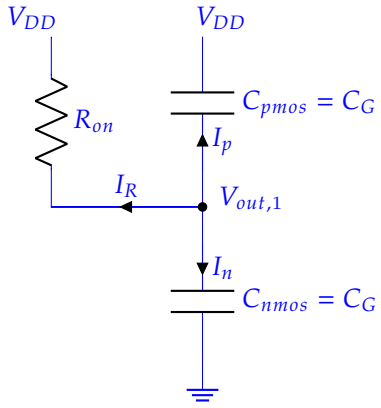


Figure 7: Inverter output at 1

This time, both I_R and I_p will affect the amount of charged pulled out of V_{DD}.

$$I_R = \frac{V_{out,1}(t) - V_{DD}}{R_{on}} = \frac{V_{DD}\left(1 - e^{-\frac{t}{2R_{on}C_G}}\right) - V_{DD}}{R_{on}} = \frac{-V_{DD}e^{-\frac{t}{2R_{on}C_G}}}{R_{on}}$$
$$I_p = C_G\frac{d}{dt}(V_{out,1}(t) - V_{DD}) = -C_G\frac{-1}{2C_GR_{on}}V_{DD}e^{-\frac{t}{2C_GR_{on}}}$$

Thus:

$$\begin{aligned} Q_{1\to 0} &= \int_0^\infty I_P(t) + I_R(t)dt = \int_0^\infty -C_G\frac{-1}{2C_GR_{on}}V_{DD}e^{-\frac{t}{2C_GR_{on}}} + \frac{-V_{DD}e^{-\frac{t}{2R_{on}C_G}}}{R_{on}}dt \\ &= -C_GV_{DD}e^{-\frac{t}{2C_GR_{on}}}|_0^\infty + \frac{-V_{DD}}{R_{on}} \cdot -1 \cdot 2R_{on}C_Ge^{-\frac{t}{2R_{on}C_G}}|_0^\infty \\ &= -C_GV_{DD}(0-1) + 2C_GV_{DD}(0-1) \\ &= -C_GV_{DD} \end{aligned}$$

The total charge is thus

$$Q_{total} = Q_{0\to 1} + Q_{1\to 0} = -C_GV_{DD} - C_GV_{DD} = -2C_GV_{DD}$$

Note that the current direction for I_p and I_R were pointing into the V_{DD} source, so the charge represents the charge moved **into** the power supply. As the question asks for the charge pulled out of the power supply, we know:

$$Q_{\text{pulled out of power supply}} = -Q_{total} = 2C_GV_{DD} = 2(1\text{fF} \cdot 1\text{V}) = 2\text{fC}$$

4 CMOS Scaling

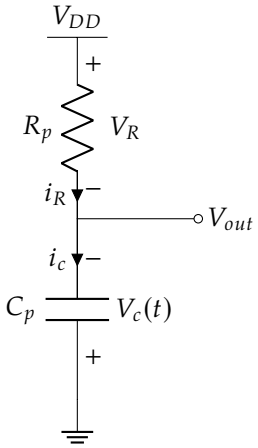
Jerry wants to create a new machine learning accelerator chip using CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transitions and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate). These two parameters are very important for CMOS technology, as they determine how quickly the processor can run and how much power it will consume.

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1\text{V}$. The transistors have a parasitic resistance of $R_p = 10\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5\text{fF}$.

Process B uses a supply voltage of $V_{DD} = 3\text{V}$. The transistors have a parasitic resistance of $R_p = 30\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1\text{fF}$.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:



Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

a) In terms of the variables V_{DD}, R_p, and C_p, **solve for** $V_{out}(t)$.

Solution

To find an expression for $V_{out}(t)$:

$$V_c(t) = V_{out}(t)$$

KCL at V_{out} (note the direction of i_R) yields:

$$i_R(t) = i_c(t)$$

$$\frac{V_{DD} - V_{out}(t)}{R_p} = C_p \frac{dV_{out}(t)}{dt}$$

$$\frac{dV_{out}(t)}{dt} + \frac{1}{R_p C_p} V_{out}(t) = \frac{V_{DD}}{R_p C_p}$$

We can either guess and check or use substitution of variables to get the solution

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)$$

b) Using the expression for $V_{out}(t)$ that was just calculated, **solve for** $i_R(t)$. Keep this expression in terms of the variables V_{DD}, R_p, and C_p.

Solution

$$i_R(t) = \frac{V_{DD} - V_{out}(t)}{R_p} = \frac{V_{DD} - V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)}{R_p} = \frac{V_{DD} e^{-\frac{t}{R_p C_p}}}{R_p}$$

c) In the previous part, you should have noticed that $i_R(t)$ started at some value, and decayed towards 0 as $t \to \infty$.

Why does this trend make sense? If the voltage were switching to a different level, would the same trend in current hold?

Solution

In steady state (i.e. when $t \to \infty$), we know that the voltage will settle to a constant value. Because $i_C = C\frac{dV_C}{dt}$, it makes sense that when the voltage is constant, the current through the capacitor will be 0. In general, this trend will hold true: when there is a step voltage change (in this case, the transistor suddenly switching on/off) in a circuit with a resistor and capacitor, the current through capacitor will jump to some level ($i_0 = i(t = 0)$), and will then exponentially decay to reach a steady state current of 0.

d) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the time it takes for** V_{out} **to reach** $\frac{V_{DD}}{2}$.

Solution

We can find the delay time by setting $V_{out}(t) = \frac{V_{DD}}{2}$:

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t}{R_p C_p}}\right)$$

$$\frac{1}{2} = e^{-\frac{t}{R_p C_p}}$$

$$\ln\left(\frac{1}{2}\right) = -\frac{t}{R_p C_p}$$

$$t = -\ln\left(\frac{1}{2}\right) R_p C_p$$

From this, we can say that the delay time to reach $\frac{V_{DD}}{2}$ for any R_p and C_p is:

$$t_d = 0.69 R_p C_p$$

$$t_d = 0.69(10 \times 10^3 \times 5 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

e) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}.**

For this problem, recall that the instantaneous power delivered by a voltage source is $P(t) = I(t) \cdot V(t)$. Note that the current and voltage are functions of time.

Energy can be found by integrating power:

$$E = \int_{t=0}^{t=\infty} P(t)dt$$

Remember that the units of energy are Joules [J], while the units of power are Watts [W], which is energy per time: $1\text{W} = \frac{1\text{J}}{1\text{s}}$

Solution

The total energy delivered by the source can be found by integrating the instantaneous power:

$$U_s = \int_0^\infty P(t)dt = \int_0^\infty V_{DD} i_R(t)dt$$

$$i_R(t) = C_p \frac{dV_{out}(t)}{dt}$$

$$i_R(t) = C_p V_{DD} \frac{1}{R_p C_p} e^{-\frac{t}{R_p C_p}} = \frac{V_{DD}}{R_p} e^{-\frac{t}{R_p C_p}}$$

$$U_s = \int_0^\infty (V_{DD}) \left(\frac{V_{DD}}{R_p} e^{-\frac{t}{R_p C_p}} \right) dt$$

$$U_R = \int_0^\infty \frac{V_{DD}^2}{R_p} e^{-\frac{t}{R_p C_p}} dt$$

$$U_s = \left(\frac{V_{DD}^2}{R_p} \right) \left(-R_p C \right) e^{-\frac{t}{R_p C_p}} \Bigg|_0^\infty$$

The total energy supplied by the supply when charging up the capacitor is:

$$U_s = C V_{DD}^2$$

Plugging in component values of process A for the energy dissipation and time delay:

$$U_s = (5 \times 10^{-15}) 1^2 = 5 \times 10^{-15}\text{J}$$

Note: Notice that the energy supplied by the supply when charging the capacitor is $U_s = CV_{DD}^2$. However, we know that the energy stored by a capacitor is $U_{cap} = \frac{1}{2} C V_{DD}^2$.

This implies that the energy drawn from the supply in charging the capacitor is twice the energy that the capacitor finally stores when it is charged. Where did the other half of the energy go? It is dissipated as heat through the resistor when charging the capacitor. If you do a similar calculation to what you just did, where you integrate the energy dissipated through the resistor as the capacitor is charging (i.e. apply $P = I \cdot V$ to the resistor and integrate), you will find the missing half of the energy.

f) **Repeat parts (d) and (e), but with the values from process B.**

Solution

Using the equations derived above:

$$U_s = (1 \times 10^{-15})3^2 = 9 \times 10^{-15}\text{J}$$

$$t_d = 0.69(30 \times 10^3 \times 1 \times 10^{-15}) = 2.07 \times 10^{-11}\text{s}$$

g) **Compare the energy and delay of process A and B.**

Solution

Compared to process B, process A dissipates less energy per transition, but has a longer delay time.

h) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to $50\text{k}\Omega$. **Calculate the new delay and energy.**

Solution

$$U_s = (1 \times 10^{-15})2^2 = 4 \times 10^{-15}\text{J}$$

$$t_d = 0.69(50 \times 10^3 \times 1 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

i) Based on your previous answers, **which process should Jerry choose to use? Why?**

Solution

With the new V_{DD} and R_p of process B, it ends up that process B and process A have the same delay time. However, process B dissipates less energy per transition with the new V_{DD} and R_p, which means Jerry should choose process B which uses the reduced V_{DD}.

5 Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student!
We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

a) **What sources (if any) did you use as you worked through the homework?**

b) **If you worked with someone on this homework, who did you work with?**
List names and student ID's. (In case of homework party, you can also just describe the group.)

c) **Roughly how many total hours did you work on this homework?**

d) **Do you have any feedback on this homework assignment?**