1 Inverter, Capacitor, and Delay

We will now work towards understanding delays in digital circuits. Here, we consider a circuit where the output node V_{out} of an inverter is connected to a capacitor. Such capacitance is often used to model other logic gates or transistors being driven by, or *loading* the inverter. In the absence of such a capacitive load, the output of the inverter V_{out} switches immediately after the input V_{in} switches.

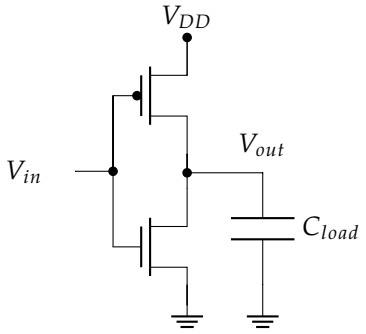
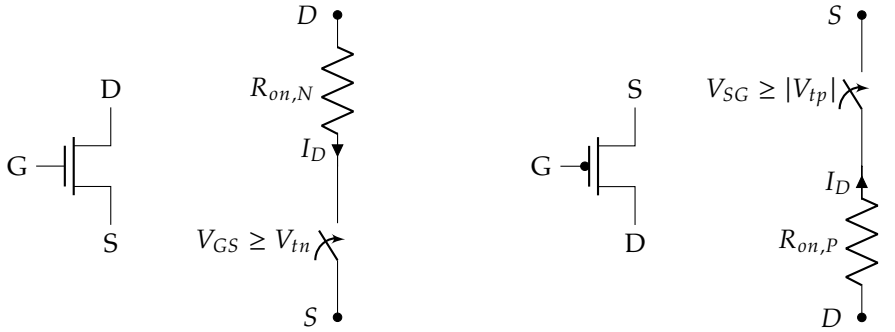


Figure 1: CMOS Inverter driving a capacitive load.

In this problem, we will be using the resistor-switch model of a transistor for analysis. These models have been shown here for your reference. Furthermore, the threshold voltages for the transistors are $V_{tn} = \frac{V_{DD}}{10}$ and $V_{tp} = \frac{-V_{DD}}{10}$.



(a) NMOS (b) PMOS

Figure 2: Transistor Resistor-switch models for NMOS and PMOS transistors.

a) Assume that V_{in} is held at 0 for a long time and then, at time t_0, it is switched to V_{DD}. Draw equivalent circuits before and after t_0 using the resistor switch model for the transistors in the inverter.

b) What is the state of the capacitor C_{load} at $t = t_0$? Will it charge or discharge from this point on?

c) Write out a differential equation governing the evolution of V_{out} after t_0. How long will it take after t_0 for the output voltage V_{out} to drop below $V_{tn} = \frac{V_{DD}}{10}$ so that a subsequent NMOS transistor will switch from on to off?

2 Differential equations with piecewise constant inputs

Let $x(\cdot)$ be a solution to the following differential equation:

$$\frac{\mathrm{d}}{\mathrm{d}t} x(t) = \lambda \left(x(t) - u(t) \right). \tag{1}$$

Let $T > 0$. Let $x[\cdot]$ "sample" $x(\cdot)$ as follows:

$$x[n] = x(nT). \tag{2}$$

Assume that $u(\cdot)$ is constant between samples of $x(\cdot)$, i.e.

$$u(t) = u[n] \quad \text{when} \quad nT \leq t < (n+1)\,T. \tag{3}$$

The above described system can be seen as an RC circuit with piecewise constant voltage applied where $\lambda = -\frac{1}{RC}$ and $u[n] = V_{in}(t)$ is kept constant when $nT \leq t < (n+1)T$.

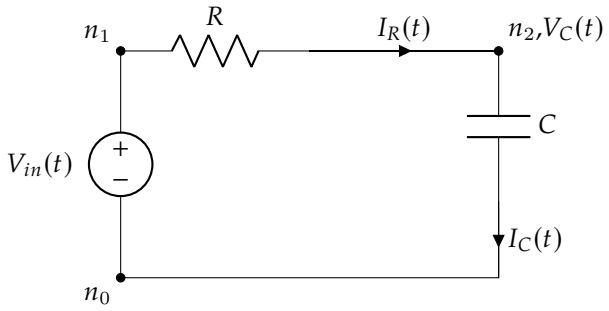


Figure 3: Example Circuit

The solution for the above system is therefore given by

$$x(nT+\tau) = e^{\lambda\tau}x[n] + (1-e^{\lambda\tau})u[n] \quad \text{for any } n \text{ and } \; 0 \leq \tau < T. \tag{4}$$

From the solution above, the relation between $x[n]$ and $x[n+1]$ is given by

$$x[n+1] = e^{\lambda T}x[n] + (1-e^{\lambda T})u[n].$$

a) Solve differential equation (1) for $nT \leq t \leq (n+1)T$ with the initial condition $x(nT) = x[n]$ and $u(t) = u[n]$ for $nT \leq t \leq (n+1)T$. Show that the solution is exactly (4).

b) Let $T = 1$ and $\lambda = -100$. Sketch a piecewise constant input $u[\cdot]$ of your choice, then sketch $x(t)$. Mark $x[n]$. Your sketch doesn't have to be exact, but you should be able to supply analysis to

justify why it looks a certain way: how are you using the fact that λT is large and negative?

c) Let $T = 1$ and $\lambda = -1$. Define $u[n]$ as follows:

$$u[n] = \begin{cases} 1, & n \text{ is even} \\ -1, & n \text{ is odd} \end{cases}. \tag{5}$$

Sketch $x(t)$.

3 A circuit with two capacitors

Consider the following circuit given in Figure 4. The devices are set to the following values: $C_1 = 1\mu F, C_2 = \frac{1}{3}\mu F,\ R_1 = \frac{1}{3}M\Omega, R_2 = \frac{1}{2}M\Omega$.

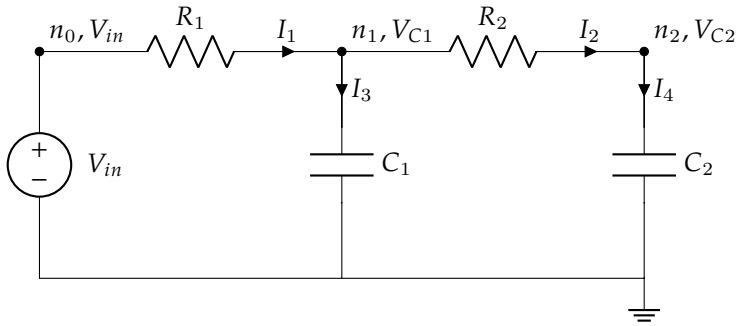


Figure 4: Two dimensional system: a circuit with two capacitors, like the one in lecture.

a) Write the differential equations for the circuit above with the variables being V_{C1} and V_{C2}. The result should only contain V_{C1}, V_{C2} and V_{in} with capacitance and resistance plugged in with their values given above.