1 Inverter, Capacitor, and Delay

We will now work towards understanding delays in digital circuits. Here, we consider a circuit where the output node V_{out} of an inverter is connected to a capacitor. Such capacitance is often used to model other logic gates or transistors being driven by, or *loading* the inverter. In the absence of such a capacitive load, the output of the inverter V_{out} switches immediately after the input V_{in} switches.

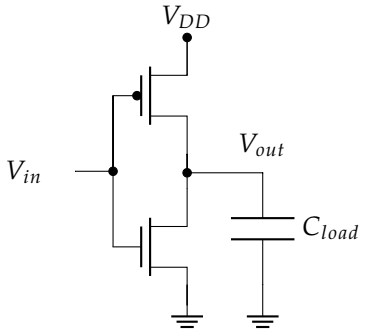
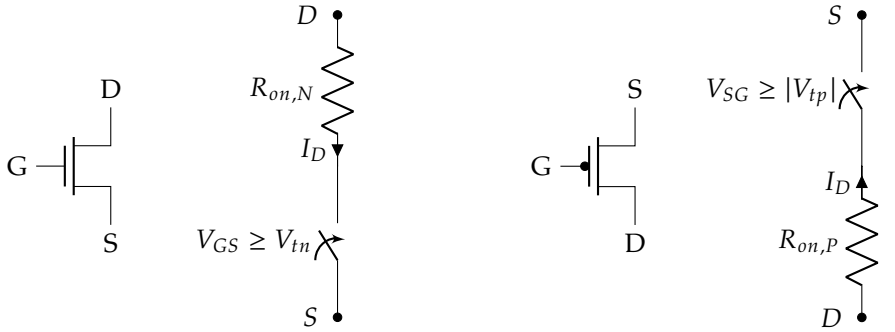


Figure 1: CMOS Inverter driving a capacitive load.

In this problem, we will be using the resistor-switch model of a transistor for analysis. These models have been shown here for your reference. Furthermore, the threshold voltages for the transistors are $V_{tn} = \frac{V_{DD}}{10}$ and $V_{tp} = \frac{-V_{DD}}{10}$.



(a) NMOS (b) PMOS

Figure 2: Transistor Resistor-switch models for NMOS and PMOS transistors.

a) Assume that V_{in} is held at 0 for a long time and then, at time t_0, it is switched to V_{DD}. Draw equivalent circuits before and after t_0 using the resistor switch model for the transistors in the inverter.

Answer

Immediately before t_0,

$$\begin{aligned} V_{GS,NMOS} &= V_{G,NMOS} - V_{S,NMOS} \\ &= V_{in} - 0 \\ &= 0 \\ V_{SG,PMOS} &= V_{S,PMOS} - V_{G,PMOS} \\ &= V_{DD} - V_{in} \\ &= V_{DD} \end{aligned}$$

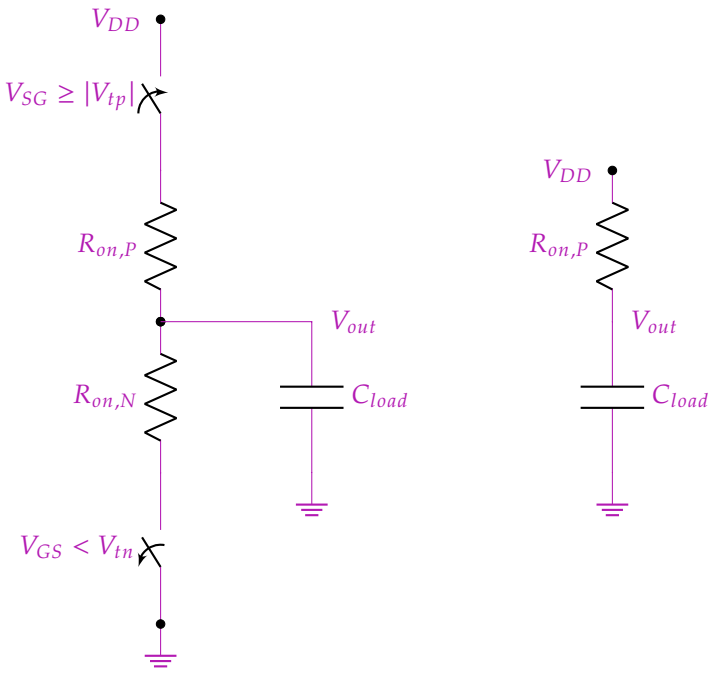


Figure 3: Equivalent circuit before t_0.

After t_0,

$$\begin{aligned} V_{GS,NMOS} &= V_{G,NMOS} - V_{S,NMOS} \\ &= V_{in} - 0 \\ &= V_{DD} \\ V_{SG,PMOS} &= V_{S,PMOS} - V_{G,PMOS} \\ &= V_{DD} - V_{in} \\ &= 0. \end{aligned}$$

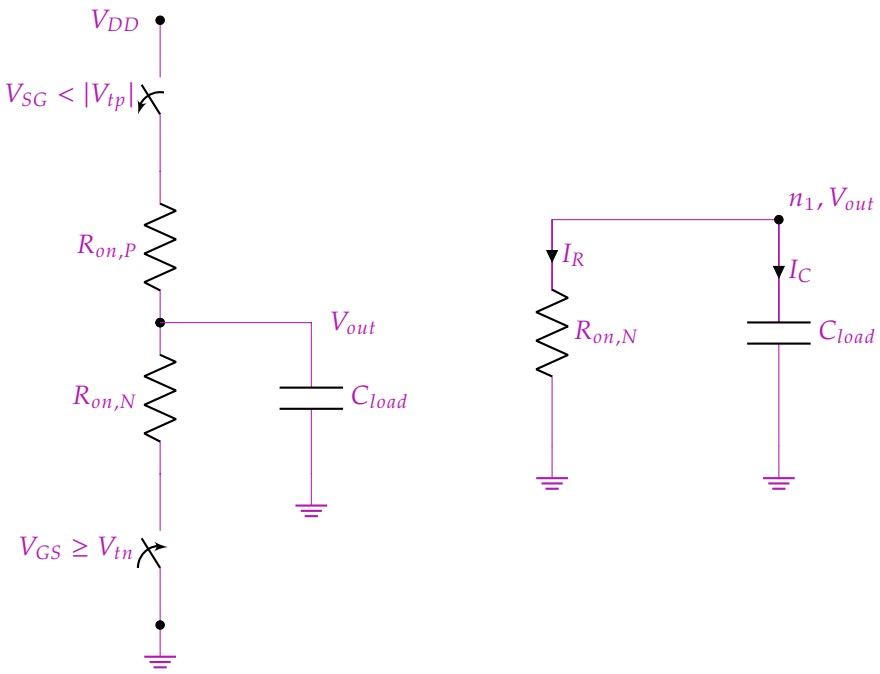


Figure 4: Equivalent circuit after t_0.

b) What is the state of the capacitor C_{load} at $t = t_0$? Will it charge or discharge from this point on?

Answer

Following the equivalent circuit representation from Figure 3, the capacitor C_{load} is charged to a voltage V_{DD}. After t_0, it will discharge to a final voltage of 0.

c) Write out a differential equation governing the evolution of V_{out} after t_0. How long will it take after t_0 for the output voltage V_{out} to drop below $V_{tn} = \frac{V_{DD}}{10}$ so that a subsequent NMOS transistor will switch from on to off?

Answer

Suppose we use $I_R(t)$ to represent the current flowing from Drain to Source for the NMOS after t_0. Also suppose the charge on the capacitor C_{load} be $Q(t)$, then $Q(t)$ and $I_C(t)$ is related such that $I_C(t)$ contributes the charge difference on the capacitor. Thus, the relation between $I_C(t)$, $Q(t)$, and $V_{out}(t)$ is

$$I_C(t) = \frac{d}{dt}Q(t)$$
$$V_{out}(t) = \frac{Q(t)}{C_{load}}.$$

KCL at node n_1 tells us

$$I_C(t) = -I_R(t).$$

Also from Ohm's law,

$$V_{out}(t) = I_R(t)R_{on,N}.$$

Combine the above equations and eliminate $I_R(t)$, $I_C(t)$ and $Q(t)$, we obtain the following differential equation:

$$\frac{d}{dt}V_{out}(t) = -\frac{V_{out}(t)}{R_{on,N}C_{load}}.$$

The solution is thus:

$$\begin{aligned} V_{out}(t) &= V_{out}(t_0)e^{-\frac{t-t0}{R_{on,N}C_{load}}} \\ &= V_{DD}e^{-\frac{t-t0}{R_{on,N}C_{load}}} \end{aligned}$$

For $V_{out}(t) = V_{tn} = \frac{V_{DD}}{10}$, the time elapsed $t - t_0$ is then,

$$\begin{aligned} t - t_0 &= -R_{on,N}C_{load}ln\left(\frac{V_{tn}}{V_{DD}}\right) \\ &= R_{on,N}C_{load}ln\left(\frac{V_{DD}}{V_{tn}}\right) \\ &= R_{on,N}C_{load}ln(10). \end{aligned}$$

2 Differential equations with piecewise constant inputs

Let $x(\cdot)$ be a solution to the following differential equation:

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \lambda\left(x(t) - u(t)\right). \tag{1}$$

Let $T > 0$. Let $x[\cdot]$ "sample" $x(\cdot)$ as follows:

$$x[n] = x(nT). \tag{2}$$

Assume that $u(\cdot)$ is constant between samples of $x(\cdot)$, i.e.

$$u(t) = u[n] \quad \text{when} \quad nT \le t < (n+1)T. \tag{3}$$

The above described system can be seen as an RC circuit with piecewise constant voltage applied where $\lambda = -\frac{1}{RC}$ and $u[n] = V_{in}(t)$ is kept constant when $nT \le t < (n+1)T$.

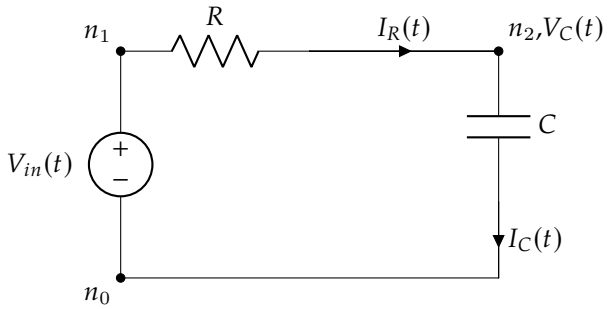


Figure 5: Example Circuit

The solution for the above system is therefore given by

$$x(nT+\tau) = e^{\lambda\tau}x[n] + (1-e^{\lambda\tau})u[n] \quad \text{for any } n \text{ and } \ 0 \le \tau < T. \tag{4}$$

From the solution above, the relation between $x[n]$ and $x[n+1]$ is given by

$$x[n+1] = e^{\lambda T}x[n] + (1-e^{\lambda T})u[n].$$

a) Solve differential equation (1) for $nT \le t \le (n+1)T$ with the initial condition $x(nT) = x[n]$ and $u(t) = u[n]$ for $nT \le t \le (n+1)T$. Show that the solution is exactly (4).

Answer

The differential equation writes

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \lambda(x(t) - u[n]).$$

Let $z(t) = x(t) - u[n]$, then since $\frac{\mathrm{d}}{\mathrm{d}t}(x(t) - u[n]) = \frac{\mathrm{d}}{\mathrm{d}t}x(t)$, we have

$$\frac{\mathrm{d}}{\mathrm{d}t}z(t) = \lambda z(t).$$

The solution is therefore

$$z(t) = Ae^{\lambda t},$$

where $A = (x(nT) - u[n])e^{-\lambda nT}$ by plugging in the initial condition $z(nT) = x(nT) - u[n]$. Thus $x(t)$ is given by

$$\begin{aligned} x(t) &= Ae^{\lambda t} + u[n] \\ &= (x(nT) - u[n])e^{-\lambda nT}e^{\lambda t} + u[n] \\ &= x(nT)e^{\lambda(t-nT)} + (1 - e^{\lambda(t-nT)})u[n]. \end{aligned}$$

Let $\tau = t - nT$ and plug in $x(nT) = x[n]$, we arrive at

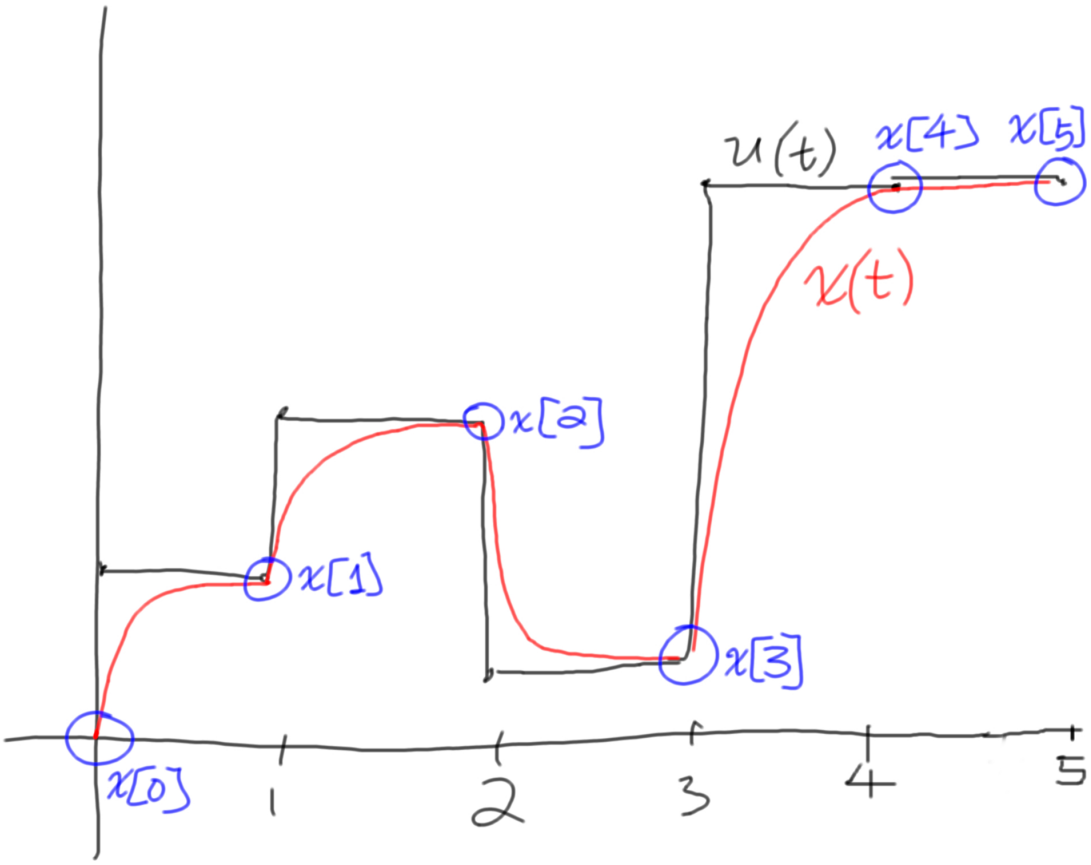
$$x(nT+\tau) = e^{\lambda\tau}x[n] + (1-e^{\lambda\tau})u[n], \quad 0 \le \tau < T.$$

The above equation holds for any n since we did not assume anything about n.

b) Let $T = 1$ and $\lambda = -100$. Sketch a piecewise constant input $u[\cdot]$ of your choice, then sketch $x(t)$. Mark $x[n]$. Your sketch doesn't have to be exact, but you should be able to supply analysis to justify why it looks a certain way: how are you using the fact that λT is large and negative?

Answer

A typical drawing might look similar to this:



Notice that the displacement between $x(t)$ and its moving target $u(t)$ is always in exponential decay (it is proportional to $z(t)$). Because λT is large and negative, $e^{\lambda T} \approx 0$, so

$$x[n+1] = e^{\lambda T} x[n] + \left(1 - e^{\lambda T}\right) u[n] \tag{5}$$

$$\approx u[n] \tag{6}$$

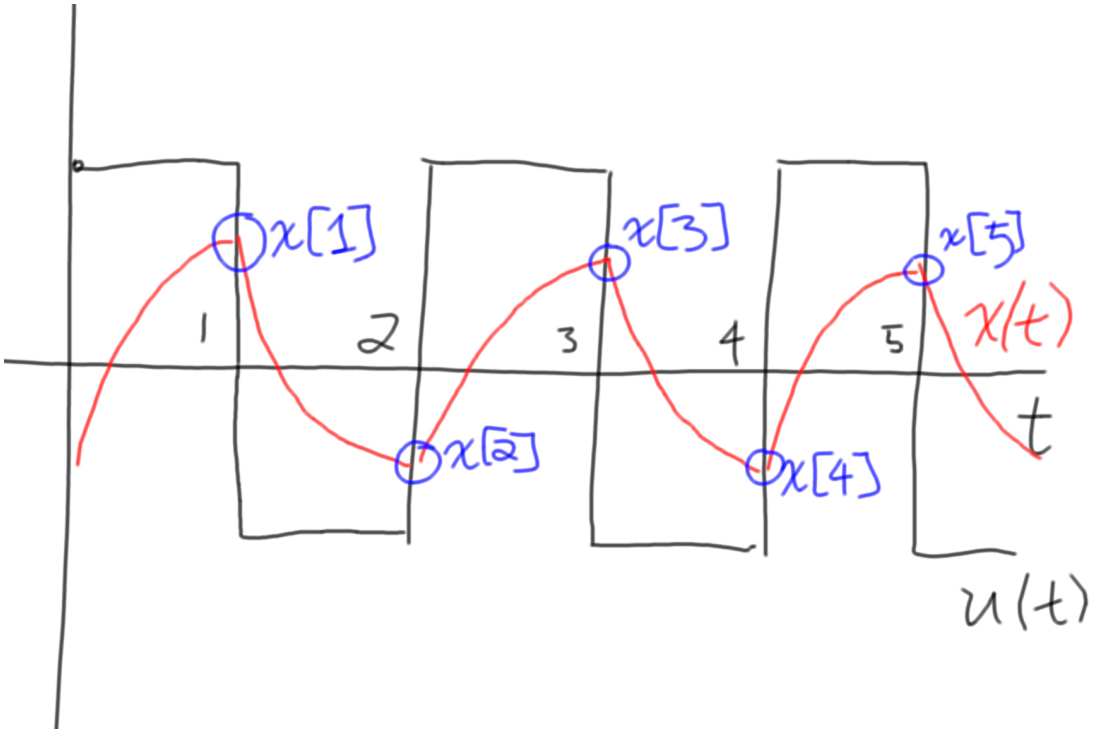
c) Let $T = 1$ and $\lambda = -1$. Define $u[n]$ as follows:

$$u[n] = \begin{cases} 1, & n \text{ is even} \\ -1, & n \text{ is odd} \end{cases}. \tag{7}$$

Sketch $x(t)$.

Answer

Notice how u, which is x's target, is flipping so quickly that x never gets close to the finish line. It gets partway there and then is told to turn around. An approximate sketch (with features exaggerated) would look like this:


x[1]
x[3]
x[5]
x(t)
1
2
3
4
5
t
x[2]
x[4]
u(t)

3 A circuit with two capacitors

Consider the following circuit given in Figure 6. The devices are set to the following values: $C_1 = 1\mu F, C_2 = \frac{1}{3}\mu F,\ R_1 = \frac{1}{3}M\Omega, R_2 = \frac{1}{2}M\Omega$.

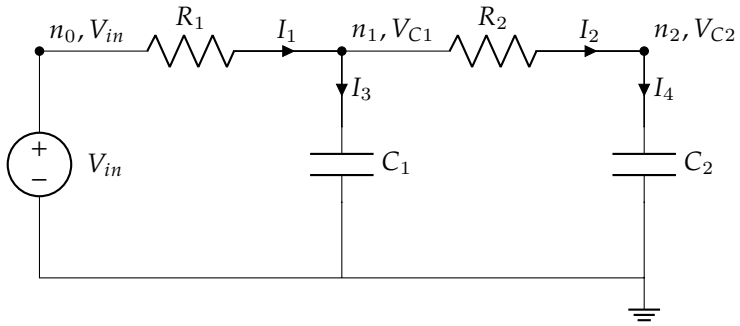


Figure 6: Two dimensional system: a circuit with two capacitors, like the one in lecture.

a) Write the differential equations for the circuit above with the variables being V_{C1} and V_{C2}. The result should only contain V_{C1}, V_{C2} and V_{in} with capacitance and resistance plugged in with their values given above.

Answer

First we note that the node potential for n_0 is V_{in}. For n_1 and n_2, we assume their potentials are V_{C1} and V_{C2} respectively. Notice that with ground as reference, V_{C1} and V_{C2} are also the capacitor voltage for C_1 and C_2. From Ohm's law, we have branch current I_1 and I_2 as follows

$$I_1 = \frac{V_{in} - V_{C1}}{R_1}$$
$$I_2 = \frac{V_{C1} - V_{C2}}{R_2}.$$

For capacitors, we have

$$V_{C1} = \frac{Q_1}{C_1}$$
$$V_{C2} = \frac{Q_2}{C_2}$$
$$C_1\frac{dV_{C1}}{dt} = \frac{dQ_1}{dt} = I_3$$
$$C_2\frac{dV_{C2}}{dt} = \frac{dQ_2}{dt} = I_4.$$

From KCL on node n_1, we have the current I_3 flowing into C_1 given by

$$I_3 = I_1 - I_2 = \frac{R_2(V_{in} - V_{C1}) - R_1(V_{C1} - V_{C2})}{R_1R_2}.$$

From KCL on node n_2, we have the current I_4 flowing into C_2 given by

$$I_4 = I_2 = \frac{V_{C1} - V_{C2}}{R_2}.$$

Rearranging a bit and plugging the current equations for I_3 and I_4 into the capacitor equations, we get:

$$\frac{dV_{C1}}{dt} = \frac{R_2(V_{in} - V_{C1}) - R_1(V_{C1} - V_{C2})}{C_1 R_1 R_2}$$
$$\frac{dV_{C2}}{dt} = \frac{V_{C1} - V_{C2}}{C_2 R_2}.$$

Plugging in the values, we arrive at:

$$\frac{dV_{C1}}{dt} = -5V_{C1} + 2V_{C2} + 3V_{in}$$
$$\frac{dV_{C2}}{dt} = 6V_{C1} - 6V_{C2}.$$