EECS 16A Designing Information Devices and Systems I
Summer 2020 Homework 4A

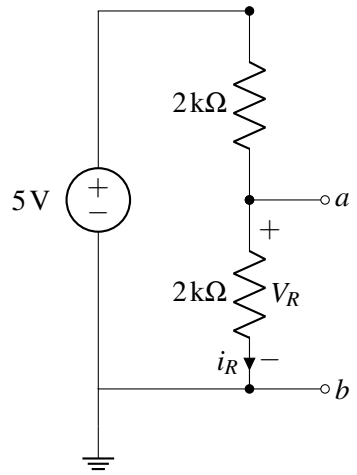
This homework is due Wednesday, July 22, 2020, at 23:59.
Self-grades are due Sunday, July 26, 2020, at 23:59.

Submission Format
Your homework submission should consist of a single PDF file that contains all of your answers (any hand-written answers should be scanned).

Homework Learning Goals: *The objective of this homework is to emphasize the importance of Thévenin equivalents in circuit analysis, and demonstrate how equivalence can help you simplify complicated resistive networks. The practice (optional) problem will introduce you to the use of capacitors as "leaky" storage elements in real world memory systems.*

1. Why Bother With Thévenin Anyway?

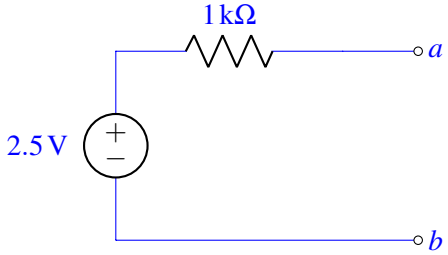
(a) Find a Thévenin eqiuvalent for the circuit shown below.



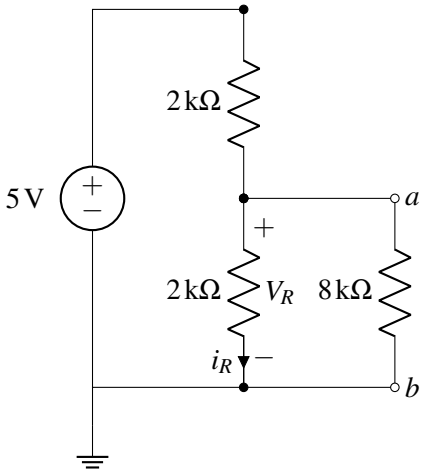
Solution:

$$V_{Th} = \frac{2\,\text{k}\Omega}{2\,\text{k}\Omega + 2\,\text{k}\Omega} \cdot 5\,\text{V} = 2.5\,\text{V}$$

$$R_{Th} = 2\,\text{k}\Omega \parallel 2\,\text{k}\Omega = 1\,\text{k}\Omega$$

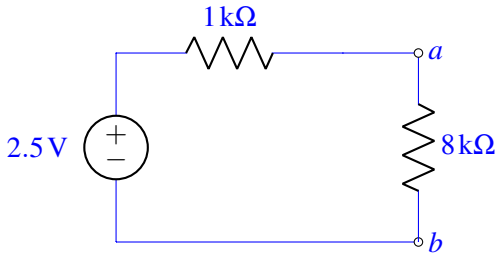


(b) What happens to the output voltage V_{ab} if we attach a load of $8\,\text{k}\Omega$ to the output as depicted in the circuit below? Use your Thévenin equivalent from part (a).



Solution:

We just attach the $8\,\text{k}\Omega$ resistor to our Thévenin equivalent circuit and calculate the voltage across it.

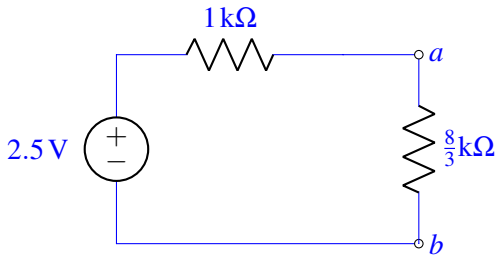


$$V_R = \frac{8\,\text{k}\Omega}{1\,\text{k}\Omega + 8\,\text{k}\Omega} \cdot 2.5\,\text{V} = 2.22\,\text{V}$$

(c) What if the load is $\frac{8}{3}\text{k}\Omega$? What if the load is $80\,\text{k}\Omega$?

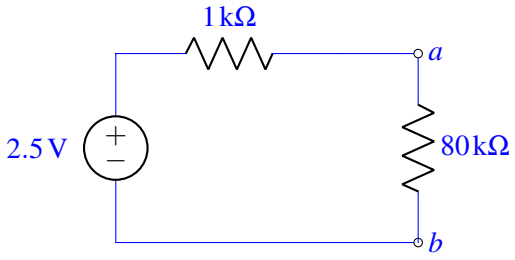
Solution:

$R = \frac{8}{3}\text{k}\Omega$:



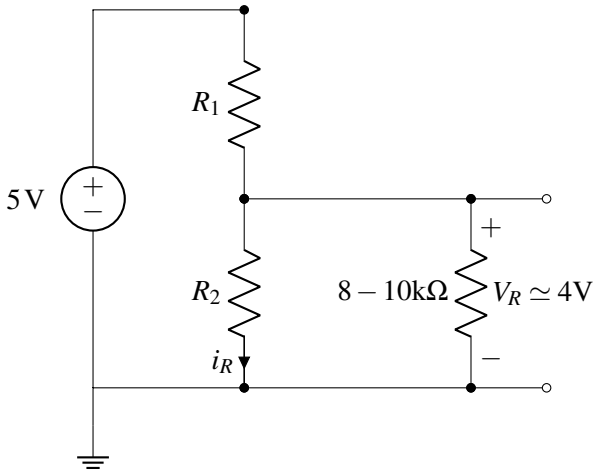
$$V_R = \frac{\frac{8}{3}\text{k}\Omega}{1\,\text{k}\Omega + \frac{8}{3}\text{k}\Omega} \cdot 2.5\,\text{V} = 1.82\,\text{V}$$

$R = 80\,\text{k}\Omega$:



$$V_R = \frac{80\,\text{k}\Omega}{1\,\text{k}\Omega + 80\,\text{k}\Omega} \cdot 2.5\,\text{V} = 2.46\,\text{V}$$

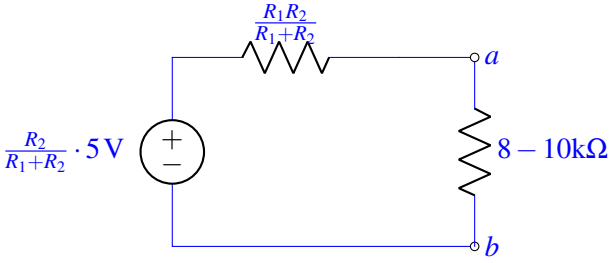
(d) Say that we want to support loads in the range of 8 kΩ to 10 kΩ. We would like to maintain 4 V across these loads. How can we approximately achieve this by setting R_1 and R_2 in the following circuit?



Solution:

$$V_{Th} = \frac{R_2}{R_1 + R_2} \cdot 5\,\text{V}$$

$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$



$$V_R = \frac{R}{R + \frac{R_1 R_2}{R_1 + R_2}} \cdot \frac{R_2}{R_1 + R_2} \cdot 5\,\text{V} \simeq 4\,\text{V}$$

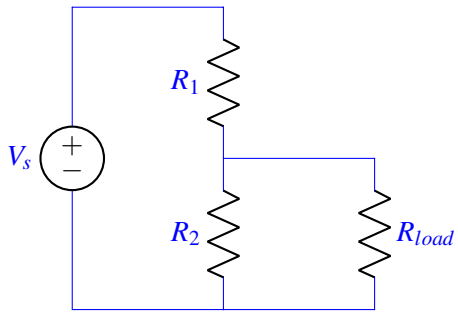
$$\frac{RR_2}{R(R_1 + R_2) + R_1 R_2} = \frac{4}{5}$$

If we set $R_1, R_2 \ll R$, then $\frac{RR_2}{R(R_1+R_2)+R_1R_2} \approx \frac{RR_2}{R(R_1+R_2)} = \frac{R_2}{R_1+R_2}$. Therefore, we can just choose two small resistors $R_1, R_2 \ll 8\,\text{k}\Omega$, such that $R_2 = 4R_1$.

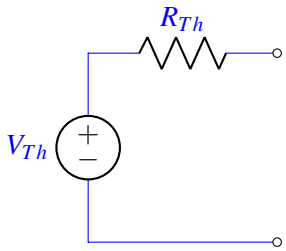
(e) For part (b), how much power does each element dissipate? Calculate the power using your Thévenin equivalent and using the original circuit. Are the values the same?

Solution:

We will ignore the power dissipated by R_{Th} initially and just explore V_s vs. V_{Th} and R_{load} in either case. This could be done for the specific example above, but it's more useful to go through this exercise generally. Thus, we will use the circuit shown below:



Recall that the Thévenin equivalent for the circuit above looks as follows:



where $R_{Th} = \frac{R_1R_2}{R_1+R_2}$ and $V_{Th} = \frac{R_2}{R_1+R_2}V_s$.

Because we are going to end up writing a few expressions multiple times, we are going to define a new variable:

$$\beta = R_1R_2 + R_{load}R_1 + R_{load}R_2$$

Let's start with our equivalent circuit. In the equivalent circuit, the current through the load resistor and equivalently every other element in the circuit is:

$$I = \frac{V_{ab}}{R_{load}} = \frac{V_{Th}}{R_{load}+R_{Th}}$$

With this current, we find the power dissapated across the source and the load resistor.

$$P_{V_{Th}} = -IV = -\frac{V_{Th}^2}{R_{load}+R_{Th}} = -\frac{V_{Th}^2(R_1+R_2)}{\beta} = -\frac{V_s^2R_2^2}{\beta(R_1+R_2)} = -0.694\,\text{mW}$$

$$P_{R_{load}} = I^2R = \frac{V_{Th}^2}{(R_{load}+R_{Th})^2}\cdot R_{load} = \frac{V_{Th}^2(R_1+R_2)^2}{\beta^2}\cdot R_{load} = \frac{V_s^2R_2^2}{\beta^2}\cdot R_{load} = 0.617\,\text{mW}$$

Let's try to find the answer from the original circuit. We will begin by calculating the current through the source.

$$I_s = \frac{V_s}{R_{eq}} = \frac{V_s}{R_1 + R_2 \parallel R_{load}} = \frac{V_s(R_1+R_2)}{\beta}$$

Now, we can calulate the power through the source.

$$P_{V_s} = -I_s V_s = -\frac{V_s^2(R_2+R_{load})}{\beta} = -6.94\,\text{mW}$$

The power dissipated by the source in the original circuit is not the same as the power dissipated in the new circuit. What about the load resistor? We will first calculate the voltage across the load resistor.

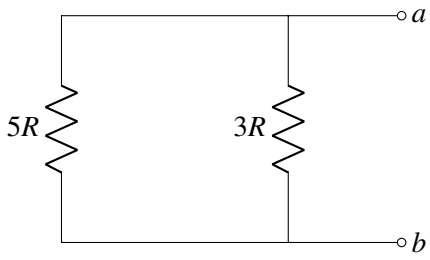
$$V_{load} = \frac{R_2 \parallel R_{load}}{R_1 + R_2 \parallel R_{load}} \cdot V_s = \frac{\frac{R_2 R_{load}}{R_2+R_{load}}}{R_1 + \frac{R_2 R_{load}}{R_2+R_{load}}} \cdot V_s = \frac{R_2 R_{load}}{\beta} \cdot V_s$$

$$P_{load} = \frac{V_{load}^2}{R_{load}} = \frac{V_s^2 R_2^2}{\beta^2} R_{load} = 0.617\,\text{mW}$$

The power through the load is the same! Thévenin equivalents can be used to calculate the power through elements that are not part of the circuit that was transformed.

2. Equivalent Resistance

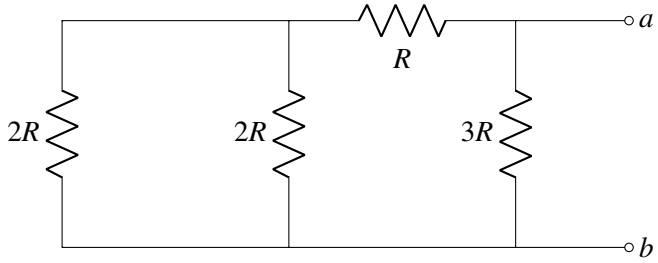
(a) Find the equivalent resistance looking in from points a and b.



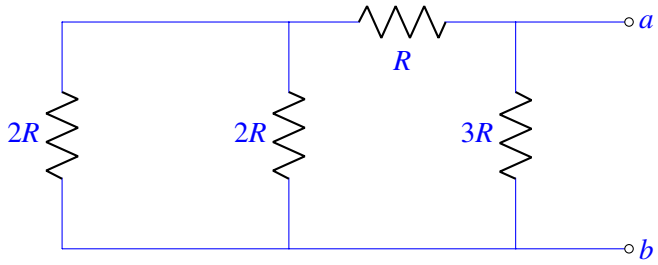
Solution:

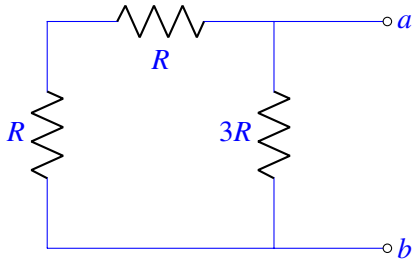
$$R_{eq} = 5R \parallel 3R = \frac{5R \cdot 3R}{5R + 3R} = \frac{15}{8}R$$

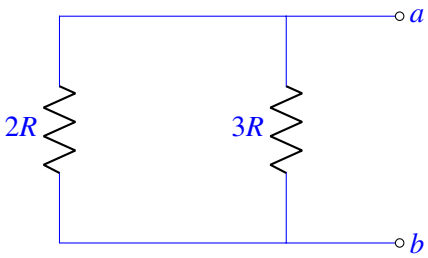
(b) Find the equivalent resistance looking in from points a and b.



Solution: We find the equivalent resistance for the resistors from left to right.

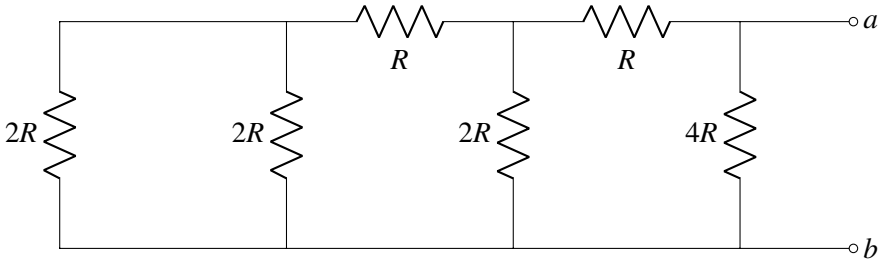




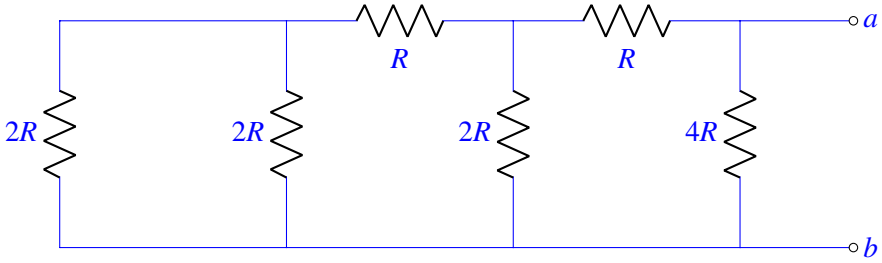


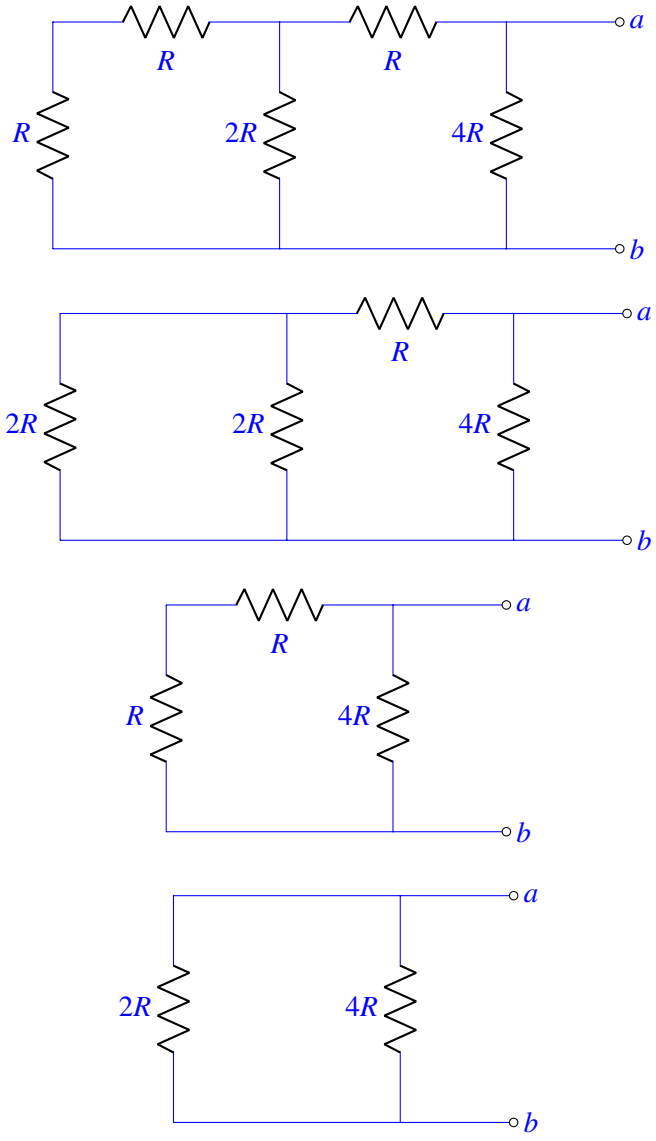
$$R_{eq} = 2R \parallel 3R = \frac{6}{5}R$$

(c) Find the equivalent resistance looking in from points a and b.



Solution: Again, we find the equivalent resistance for the resistors from left to right.





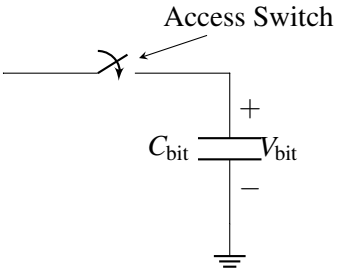
$$R_{eq} = 2R \parallel 4R = \frac{4}{3}R$$

3. Practice: Dynamic Random Access Memory (DRAM)

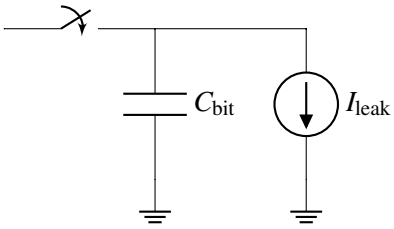
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store $>$ 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will model as a leakage to ground. The figure below shows a model of this leakage:



Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

Solution:

We want the time that a cell can read a '1' to be $t_{\text{store}} = 1\,\text{ms}$. We are given that $V_{\text{init}} = 1.2\,\text{V}$ and that $V_{\text{min}} = V_{\text{bit}} = 0.9\,\text{V}$. To get an expression for the leakage rate, we differentiate

$$Q_{\text{bit}} = V_{\text{bit}} C_{\text{bit}},$$

giving

$$I_{\text{leak}} = \frac{dV_{\text{bit}}}{dt} C_{\text{bit}}.$$

Assuming a constant leakage rate, we have

$$\begin{aligned} I_{\text{leak}} &= \frac{\Delta V_{\text{bit}}}{\Delta t} C_{\text{bit}} \\ &= \frac{V_{\text{init}} - V_{\text{min}}}{t_{\text{store}}} C_{\text{bit}}. \end{aligned}$$

Plugging in the values from above, we get

$$\begin{aligned} I_{\text{leak}} &= \frac{(1.2\,\text{V} - 0.9\,\text{V}) \cdot 28\,\text{fF}}{1 \times 10^{-3}\,\text{s}} \\ &= 8.4\,\text{pA}. \end{aligned}$$

4. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?

Solution:

I worked on this homework with...

I first worked by myself for 2 hours, but got stuck on problem 5, so I went to office hours on...

Then I went to homework party for a few hours, where I finished the homework.