EECS 16A Designing Information Devices and Systems I
Summer 2020 Homework 4A

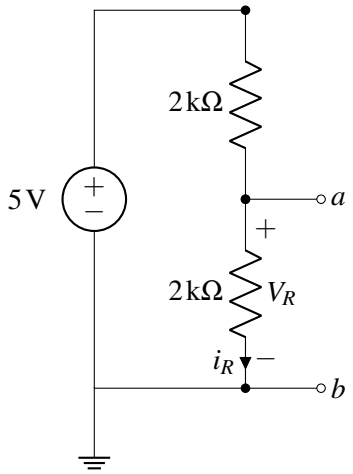
This homework is due Wednesday, July 22, 2020, at 23:59.
Self-grades are due Sunday, July 26, 2020, at 23:59.

Submission Format
Your homework submission should consist of a single PDF file that contains all of your answers (any hand-written answers should be scanned).

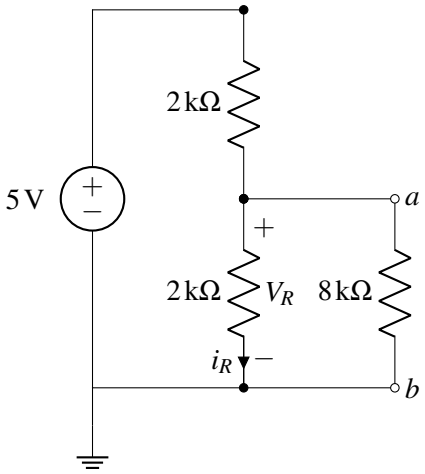
Homework Learning Goals: *The objective of this homework is to emphasize the importance of Thévenin equivalents in circuit analysis, and demonstrate how equivalence can help you simplify complicated resistive networks. The practice (optional) problem will introduce you to the use of capacitors as "leaky" storage elements in real world memory systems.*

1. Why Bother With Thévenin Anyway?

(a) Find a Thévenin eqiuvalent for the circuit shown below.

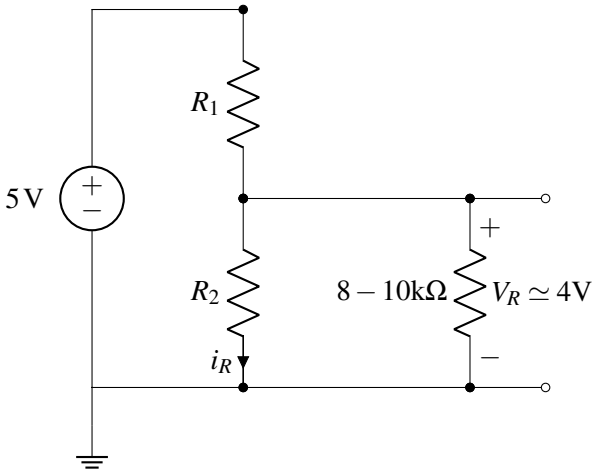


(b) What happens to the output voltage V_{ab} if we attach a load of 8 kΩ to the output as depicted in the circuit below? Use your Thévenin equivalent from part (a).



(c) What if the load is $\frac{8}{3}$kΩ? What if the load is 80 kΩ?

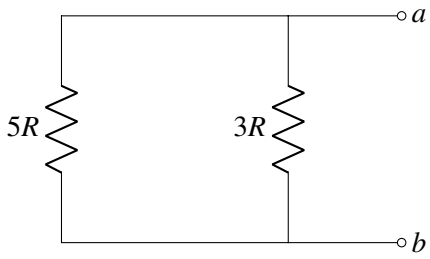
(d) Say that we want to support loads in the range of 8 kΩ to 10 kΩ. We would like to maintain 4 V across these loads. How can we approximately achieve this by setting R_1 and R_2 in the following circuit?



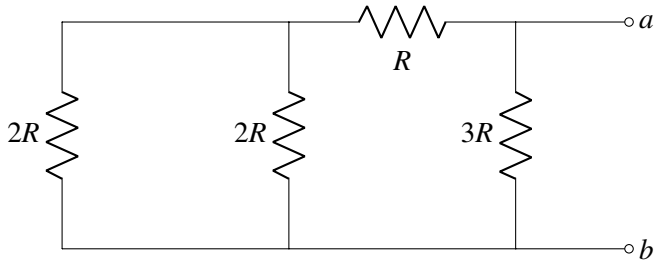
(e) For part (b), how much power does each element dissipate? Calculate the power using your Thévenin equivalent and using the original circuit. Are the values the same?

2. Equivalent Resistance

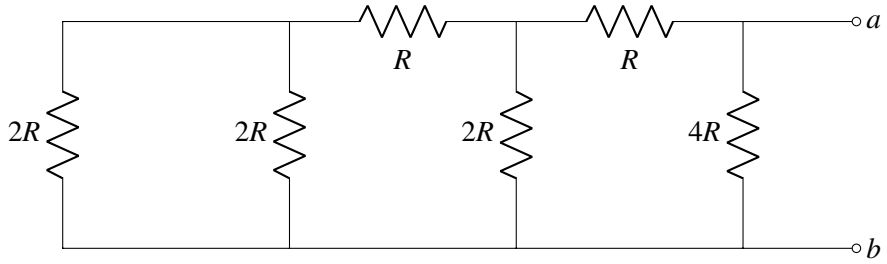
(a) Find the equivalent resistance looking in from points a and b.



(b) Find the equivalent resistance looking in from points a and b.



(c) Find the equivalent resistance looking in from points a and b.

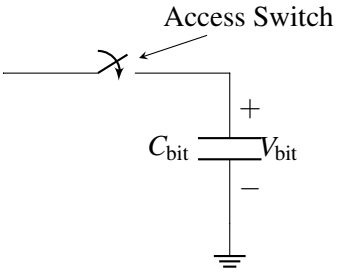


3. Practice: Dynamic Random Access Memory (DRAM)

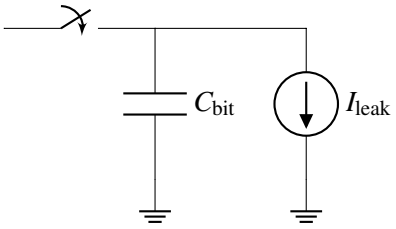
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store $>$ 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will model as a leakage to ground. The figure below shows a model of this leakage:



Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

4. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?