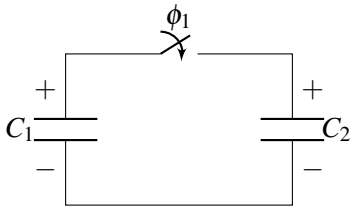
EECS 16A Designing Information Devices and Systems I
Summer 2020 Discussion 4C

1. Capacitors and Charge Conservation

(a) Consider the circuit below with $C_1 = C_2 = 1\,\mu\text{F}$ and an open switch. Suppose that C_1 is initially charged to $+1\,\text{V}$ and that C_2 is charged to $+2\,\text{V}$. How much charge is on C_1 and C_2?



Answer:

$$q_1 = C_1 V_1 = 1\,\mu\text{C}$$
$$q_2 = 2\,\mu\text{C}$$

(b) Now the switch is closed (i.e. the capacitors are connected together.) What are the voltages across and the charges on C_1 and C_2?

Answer:

Charge is always conserved.

Let $Q_{C_1,1}, Q_{C_2,1}$ be the charges on the capacitors after the switch is closed. There was $3\,\mu\text{C}$ of total charge on the top two plates of the capacitors initially, so we must have

$$Q_{C_1,1} + Q_{C_2,1} = 3\,\mu\text{C}$$

Further, the voltages on the capacitors must be the same, so:

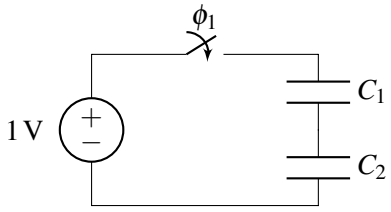
$$\frac{Q_{C_1,1}}{C_1} = \frac{Q_{C_2,1}}{C_2}$$

Solving this system gives:

$$Q_{C_1,1} = Q_{C_2,1} = 1.5\,\mu\text{C}$$

Comparing to the previous part, charge has moved from C_2 to C_1. This yields a voltage of $1.5\,\text{V}$.

(c) Consider the following circuit with $C_1 = 1\,\mu\text{F}$ and $C_2 = 3\,\mu\text{F}$. Suppose that both capacitors are initially uncharged ($0\,\text{V}$).



What are the voltages across each capacitor after the switch is closed? What are the charges on each capacitor?

Answer:

Solution 1: Use equivalent capacitance:

$$C_{eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}$$

The series has an equivalent capacitance $C_{eq} = \frac{3}{4}\mu F$, so $Q_{eq} = C_{eq}V = \frac{3}{4}\mu C$. Note that this means $+\frac{3}{4}\mu C$ is on the top plate of C_1 (and hence the top plate of C_2, etc.).

The voltage across C_1 is $\frac{Q_{eq}}{C_1} = \frac{3}{4}V$. The voltage across C_2 is $\frac{Q_{eq}}{C_2} = \frac{1}{4}V$.

Solution 2: Let an unknown $+q$ charge be on the top plate of C_1. Then by charge conservation, $-q$ charge is on the bottom plate of C_2. And since conductors have no $\vec{E}$ field, $-q$ is on the bottom plate of C_1, and $+q$ on the top of C_2.

Now, by KVL, the voltage across the series is 1 V:

$$\frac{q}{C_1} + \frac{q}{C_2} = 1\,V$$

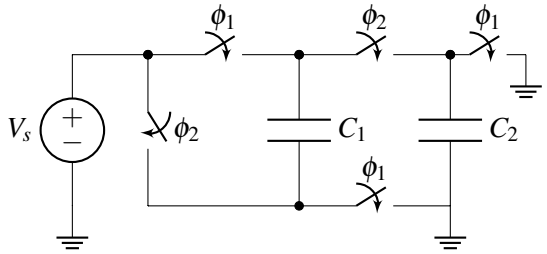
Therefore:

$$q = \frac{1\,V}{\frac{1}{C_1} + \frac{1}{C_2}}$$

Notice that we have derived the formula for equivalent capacitance of capacitors in series.

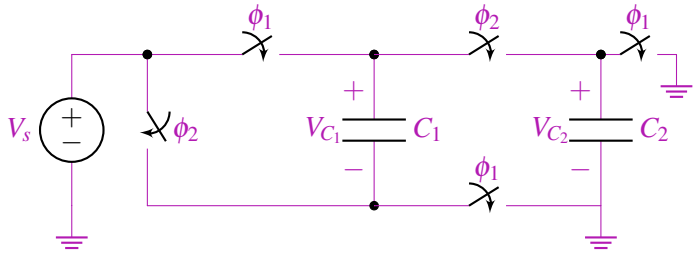
2. Charge Sharing Algorithm

For the switch capacitor circuit below, calculate the value of all node voltages at the end phase 2, as a function of the voltage source V_s and the capacitors C_1, C_2.



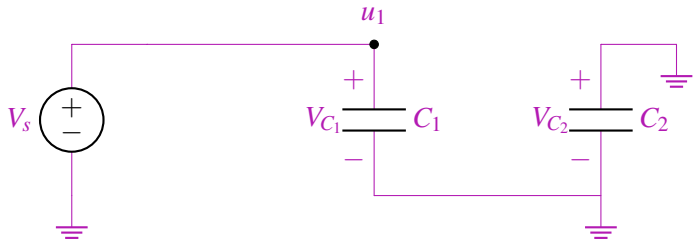
Answer:

Step 1: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "−" sign. Just make sure you stay consistent with this polarity across phases.

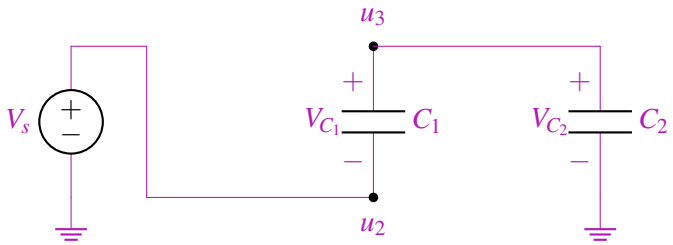


Step 2: Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the phase 1 circuit might be merged or split in phase 2.

Phase 1:



Phase 2:



Step 3: Identify all "floating" nodes in your circuit during phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.

In this case the only node that is floating during phase 2 is node u_3. (Node u_2 is connected to the voltage source, i.e. $u_2 = V_s$, and the 3^{rd} node is the ground node).

Step 4: For steps 4-6 we will **examine each phase 2 floating node individually**. Pick a floating node from the ones you found in step 3 and identify all capacitor plates connected to that node during phase 2. Then, calculate the charge on each of these plates during phase 1.
To do so, identify all nodes in your circuit during phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (step 2 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage *across* a capacitor).
Careful: The plate marked with the "$-$" sign will have $Q = -CV_C$ and the plate marked with the "$+$" sign will have $Q = CV_C$ stored onto them.
Careful 2: We assume here that you know all node voltages during phase 1. If you don't, before starting this procedure calculate the node voltages you need using one of the previously introduced circuit analysis techniques (most likely KVL will do the job).

Looking at our single floating node we can see that the "+" plates of C_1 and C_2 are connected to it during phase 2. Let's calculate the charge on these plates during **phase** ϕ_1.

$$\begin{aligned} Q_{u_3}^{\phi_1} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (V_s - 0)C_1 + 0 \\ &= V_sC_1 \end{aligned}$$

Step 5: Find the total charge on each of the floating nodes during phase 2 as a function of node voltages. Use the same process as in Step 4, but this time using the node voltages during phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

$$\begin{aligned} Q_{u_3}^{\phi_2} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (u_3 - u_2)C_1 + (u_3 - 0)C_2 \\ &= (u_3 - V_s)C_1 + u_3C_2 \end{aligned}$$

Step 6: Equate the total charge calculated in phase 1 (Step 4) to the total charge calculated in phase 2 (Step 5) (charge conservation).

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{u_3}^{\phi_2} \\ V_sC_1 &= (u_3 - V_s)C_1 + (u_3 - 0)C_2 \\ u_3 &= \frac{2C_1}{C_1 + C_2}V_s \end{aligned}$$

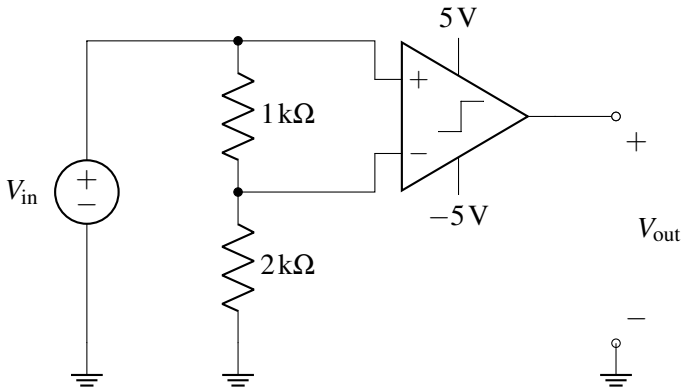
Step 7: Repeat steps 4-6 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

In this problem we did not go through step 7 since we only had one floating node during phase 2. This means we have only one unknown node voltage (u_3) for which we solved using our single equation from Step 6. We will be using step 7 in our second example!

3. Practice: Comparators

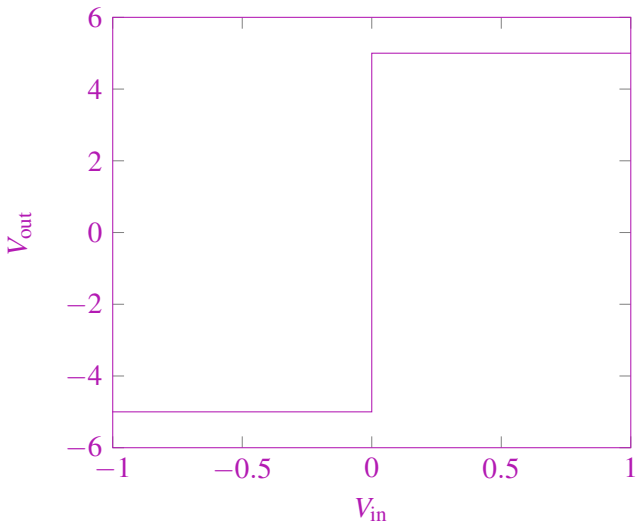
For each of the circuits shown below, plot V_{out} for V_{in} ranging from $-10\,V$ to $10\,V$ for part (a) and from $0\,V$ to $10\,V$ for part (b).

(a)

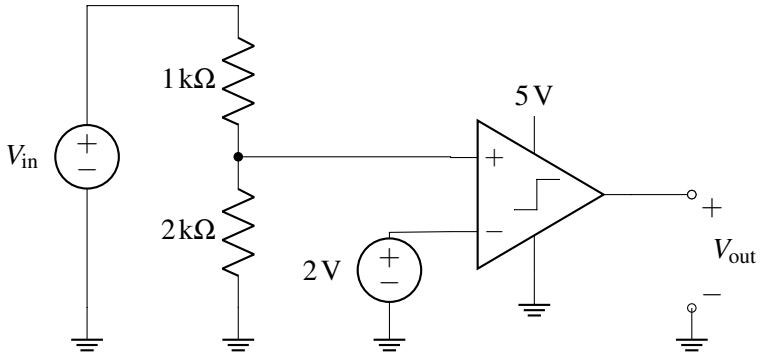


Answer:

When the positive terminal's voltage, V_+, is greater than the negative terminal's voltage, V_-, the value at the positive supply rail, V_{DD},will be output. Likewise, if the negative terminal's voltage, V_-, has a higher voltage then the value at the negative supply rail, V_{SS}, will be output. Since V_- is just the output of a voltage divider with the source $V_{in} = V_+$, it will always have lower absolute value and same polarity as the positive terminal. Thus, the comparator's output will depend only on the sign of the source V_{in}.



(b)



Answer:

$$V_+ = \frac{2\,\text{k}\Omega}{1\,\text{k}\Omega + 2\,\text{k}\Omega} V_{in} = \frac{2}{3} V_{in}$$

$$V_- = 2\,\text{V}$$

The comparator will output positive 5V when the voltage divider's output $V_+ > 2\,\text{V}$ and thus when $V_{in} > 3\,\text{V}$. Otherwise, it will output 0V (ground).