EECS 16A Designing Information Devices and Systems I
Spring 2022 Homework 10

This homework is due April 8, 2022, at 23:59.
Self-grades are due April 11, 2022, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw10.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. **Reading Assignment**

No submission is required for this problem, however we ask that you read and understand the notes.

For this homework, please read Note 17A to learn about comparators and op-amps, and Note 17B to learn about charge sharing. You are always encouraged to read beyond this as well.

(a) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what is the minimum/maximum value of V_{out}?

(b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

Solution:

a) The minimum op-amp output will always be the value of the V_{SS} supply rail, and thus 0V in this case. The maximum op-amp output will always be the value of the V_{DD} supply rail, and thus 5V in this case.

b) A comparator gives a binary output of either a high value or a low value depending on the difference of voltage between its two input terminals. Thus, comparators can be used as indicators or switches. In the case of a touchscreen, a comparator can indicate whether or not a touch occurs. This can be done by hooking up one of the comparator terminals to the equivalent capacitance of the touchscreen, and the other terminal to a reference voltage source. The value of this reference voltage source needs to be between the peak of the voltage over the capacitor with and without touch. Thus, when a touch occurs, the difference between the input terminals will invert in sign, and the comparator will respond.

2. **Fun With Charge Sharing**

(a) Capacitors C_1 and C_2 are charged to V_1 and V_2 and switch S_1 is open for time $t < 0$. At time $t = 0$, switch S_1 is closed. Calculate V_1 at time $t > 0$.
Use the following values: $C_1 = 1\text{F}$, $C_2 = 4\text{F}$, $V_1 = 6\text{V}$, $V_2 = 1\text{V}$.

Solution:

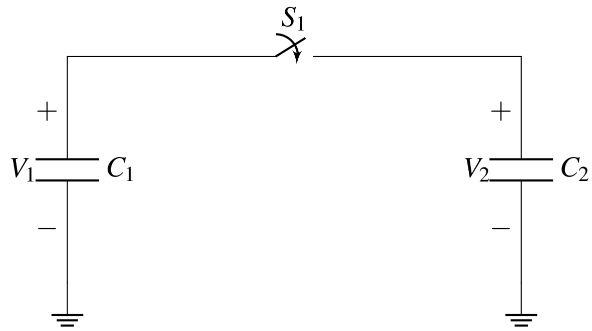


Figure 1: Capacitor Charge Sharing

Let us define the initial charge on C_1 as Q_{1i} and the initial charge on C_2 as Q_{2i}. We know that $Q_{1i} = C_1V_{1i}$ and $Q_{2i} = C_2V_{2i}$, where V_{1i} and V_{2i} are the initial voltages across C_1 and C_2, respectively. (i.e. before switch S_1 is closed). We know from conservation of charge that $Q_{1i} + Q_{2i} = Q_{1f} + Q_{2f}$, where Q_{1f} and Q_{2f} are the final charge on C_1 and C_2. (i.e. after switch S_1 is closed). We can write this as:

(1) $C_1V_{1i} + C_2V_{2i} = Q_{1f} + Q_{2f}$.

Additionally, we know that once switch S_1 is closed, the voltage across C_1 and C_2 must be the same, because they are now in parallel with each other. Specifically, $V_{1f} = V_{2f}$ where V_{1f} and V_{2f} are the final voltages across C_1 and C_2, respectively. (i.e. after switch S_1 is closed). Therefore,

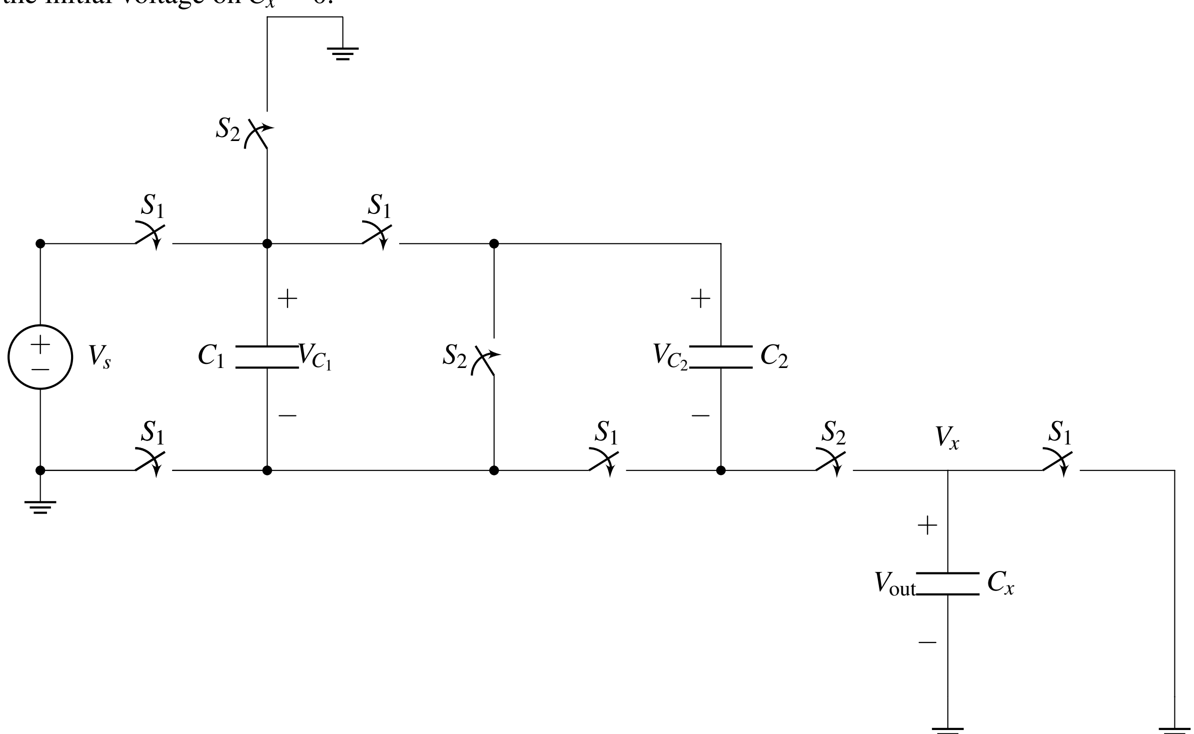
$C_1V_{1i} + C_2V_{2i} = (C_1 + C_2)V_1 f$

At time $t > 0$, $V_{1f} = V_1 = \frac{C_1V_{1i}+C_2V_{2i}}{C_1+C_2}$

Plugging in numbers, we get:

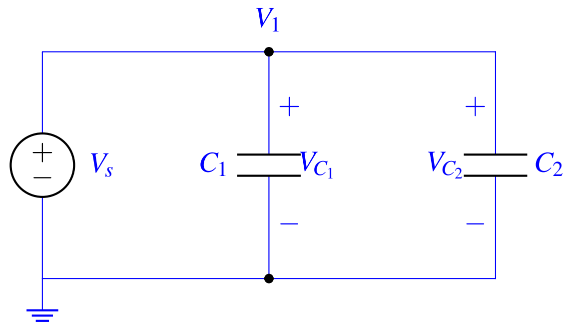
$V_{1f} = 2V$

(b) The circuit shown below operates in two phases. During phase 1, switches labeled S_1 are closed and switches S_2 are open. During phase 2, switches S_1 are open and switches S_2 are closed. Assume that the initial voltage on $C_x = 0$.



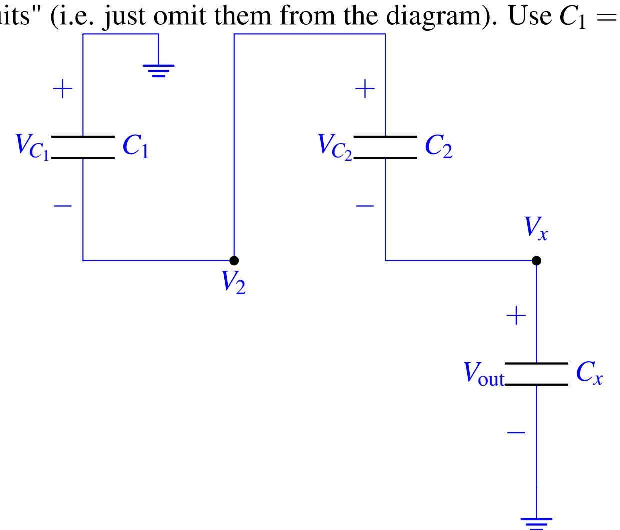
i. Redraw the circuit during phase 1. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$.

Solution:



ii. Redraw the circuit during phase 2. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$.

Solution:



iii. Calculate the value of the voltage V_{out} during phase 2 as a function of C_0, C_x, and V_s. Use $C_1 = C_2 = C_0$.

Solution: Step 1:
Identifying all floating nodes during phase 2. The floating nodes are V_2 and V_x since they are connected only to capacitor plates. No current can flow in or out of them.
Step 2:
For the V_2 node:
In phase 1, the total charge is equal to $Q_1 + Q_2 = -C_1V_s + C_2V_s$.
In phase 2, from charge conservation, we get:

$$-C_1V_s + C_2V_s = C_1V_2 + C_2(V_2 - V_{out}) \tag{1}$$

For the V_x node:
In phase 1, the charge at the bottom plate of C_2 was $-C_2V_s$ In phase 2, from charge conservation, we get:

$$-C_2V_s = C_2(V_{out} - V_2) + C_xV_{out} \tag{2}$$

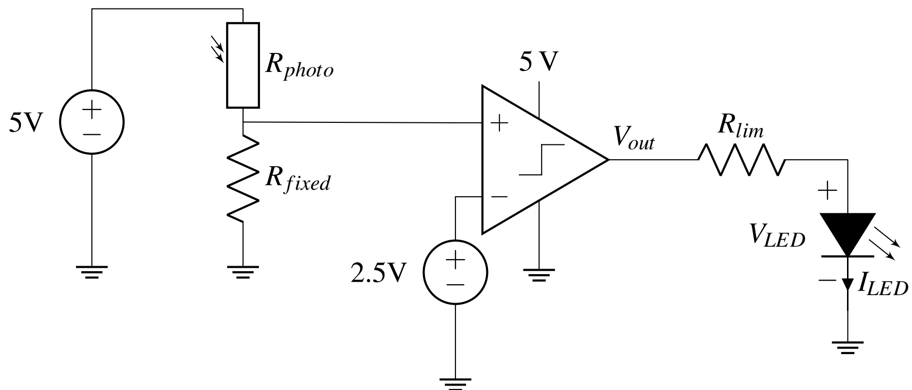
$$V_2 = \frac{(C_x + C_2)V_{out} + C_2V_s}{C_2} \tag{3}$$

Plugging (3) into (1),

$$V_{out} = \frac{-C_1C_2V_s}{C_1C_x + C_1C_2 + C_2C_x} = \frac{-V_s}{1 + \frac{2C_x}{C_0}}$$

3. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) "alarm" if the kitchen drawer is opened.



Note R_{photo} is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

V_{LED} indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is V_+, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of R_{photo} and R_{fixed}.

Solution: V_+ is the output of a voltage divider:

$$V_+ = \frac{R_{fixed}}{R_{fixed} + R_{photo}} \cdot 5\,\text{V}$$

(b) We now want to choose a value for R_{fixed}. From the photoresistor's datasheet, we see the resistance in "light" conditions (i.e. drawer open) is $1\,\text{k}\Omega$. In "dark" conditions (i.e. drawer closed), the resistance is $10\,\text{k}\Omega$.

To ensure the comparator detects the light condition with more tolerance, we decide to design R_{fixed} so that V_+ is $3\,\text{V}$ under the "light" condition. Solve for the value of R_{fixed} to meet this specification.

Solution: We start from the voltage divider equation we derived in the previous part:

$$V_+ = \frac{R_{fixed}}{R_{fixed} + R_{photo}} \cdot 5\,\text{V}$$

Now we plug in the known values, $V_+ = 3\,\text{V}$ and $R_{photo} = 1\,\text{k}\Omega$.

$$3\,\text{V} = \frac{R_{fixed}}{R_{fixed} + 1000\Omega} \cdot 5\,\text{V}$$

Solving this equation, we get $R_{fixed} = 1.5\,\text{k}\Omega$.

(c) Write down V_{out} with any conditions in terms of V_+. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

Solution:

Since the comparator is ideal, we know that V_{out} will be the voltage at either the positive rail (5 V) or at the negative rail (0 V) when $V_+ \neq V_-$. Which voltage depends on if V_+ is greater than V_- or not. Since V_- is 2.5 V, we get the following piecewise equation for V_{out}:

$$V_{out} = \begin{cases} 5\,\mathrm{V}, & V_+ > 2.5\,\mathrm{V} \\ 0\,\mathrm{V}, & V_+ < 2.5\,\mathrm{V} \end{cases}$$

(d) Using your answers to the previous parts, write down V_{out} with the conditions on its output in terms of R_{photo}. You can substitute the value of R_{fixed} you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

Solution:

We substitute the equations for V_+ into the equation for V_{out}:

$$V_{out} = \begin{cases} 5\,\mathrm{V}, & \frac{R_{fixed}}{R_{fixed}+R_{photo}} \cdot 5\,\mathrm{V} > 2.5\,\mathrm{V} \\ 0\,\mathrm{V}, & \frac{R_{fixed}}{R_{fixed}+R_{photo}} \cdot 5\,\mathrm{V} < 2.5\,\mathrm{V} \end{cases}$$

Plugging in $R_{fixed} = 1.5\,\mathrm{k\Omega}$ from part (b), we can get the following in terms of R_{photo}:

$$V_{out} = \begin{cases} 5\,\mathrm{V}, & R_{photo} < 1.5\,\mathrm{k\Omega} \\ 0\,\mathrm{V}, & R_{photo} > 1.5\,\mathrm{k\Omega} \end{cases}$$

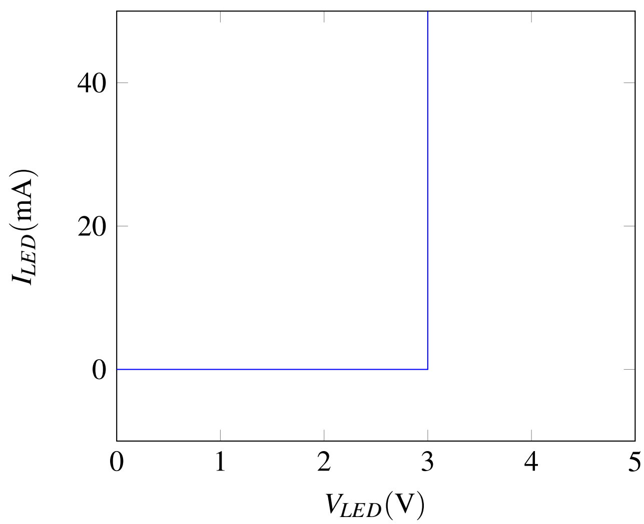
(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED's datasheet, the forward voltage, V_F is 3 V. Essentially, if V_{LED} is less than this voltage, the LED won't light up and I_{LED} will be 0 A.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

i. If the voltage across the LED is less than $V_F = 3\,\mathrm{V}$ or if $I_{LED} < 0\,\mathrm{A}$, then the LED acts like an open circuit.

ii. If the voltage across the LED is $V_F = 3\,\mathrm{V}$, then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).



To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for I_{LED} is 20 mA.

Find the value of the current-limiting resistor, R_{lim}, such that when the photoresistor is in the "light" condition, $I_{LED} = 20\,\text{mA}$.

Solution: When the photoresistor is in the "light" condition, $R_{photo} = 1\,\text{k}\Omega$, and based on our analysis in the previous part, $V_{out} = 5\,\text{V}$. This implies that $V_{LED} = V_F$ and the LED acts like a power supply with positive current flow when in the "light" condition.

Using Ohm's Law and noting that the same current passes through R_{lim} and the LED itself,

$$V_{out} - V_F = I_{LED} R_{lim}$$

Rearranging and plugging in values when in the "light" condition:

$$R_{lim} = \frac{V_{out} - V_F}{I_{LED}}$$

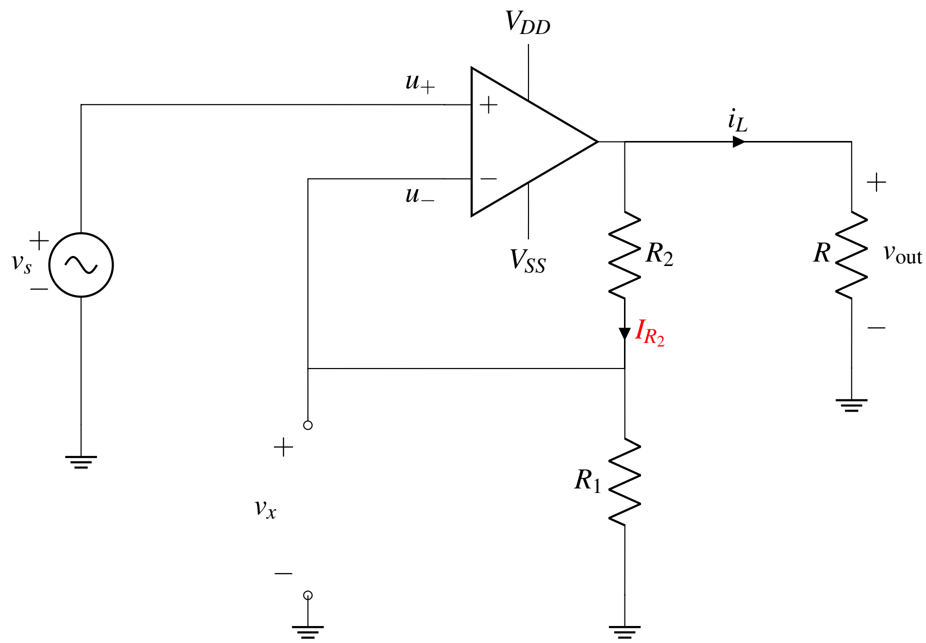
$$R_{lim} = \frac{5 - 3\text{ V}}{0.02\text{ A}}$$

$$R_{lim} = 100\,\Omega$$

Note that when $V_{out} < 3\,\text{V}$, the LED will not light up and I_{LED} will be 0 mA. Thus by our design of the voltage divider, we were able to ensure the LED lights up only if the drawer is opened.

4. Op-Amp in Negative Feedback

In this question, we analyze op-amp circuits that have finite op-amp gain A. We replace the op-amp with its circuit model with parameterized gain and observe the gain's effect on terminal and output voltages as the gain approaches infinity. **Note here that** $V_{SS} = -V_{DD}$**.**



For parts (a) - (e) only, assume that the op-amp is ideal (i.e., $A \to \infty$). We will consider the case of finite gain A in parts (f) - (h).

(a) Consider the circuit shown above and $V_{SS} = -V_{DD}$. What is $u_+ - u_-$?

Solution: For ideal op-amp circuits in negative feedback, the voltage at the two terminals must be equal, so $u_+ - u_- = 0$.

(b) Find v_x as a function of v_{out}.

Solution: We see that v_x is the middle node of a voltage divider, so $v_x = v_{out}\frac{R_1}{R_1+R_2}$.

(c) What is I_{R_2}, i.e. the current flowing through R_2 as a function of v_s? *Hint: Find the current through R_1 first.*

Solution: We know from part (a) that $v_x = v_s$. The current flowing through R_1 is $I_{R_1} = \frac{v_s}{R_1}$. This current also flows through R_2.

(d) Find v_{out} as a function of v_s.

Solution: Using the answer from the previous part, $v_{out} = v_s + R_2 I_{R_1} = v_s + R_2\frac{v_s}{R_1} = v_s\left(\frac{R_1+R_2}{R_1}\right)$.

(e) What is the current i_L through the load resistor R? Give your answer in terms of v_{out}.

Solution: The current i_L through the load is $\frac{v_{out}}{R}$.

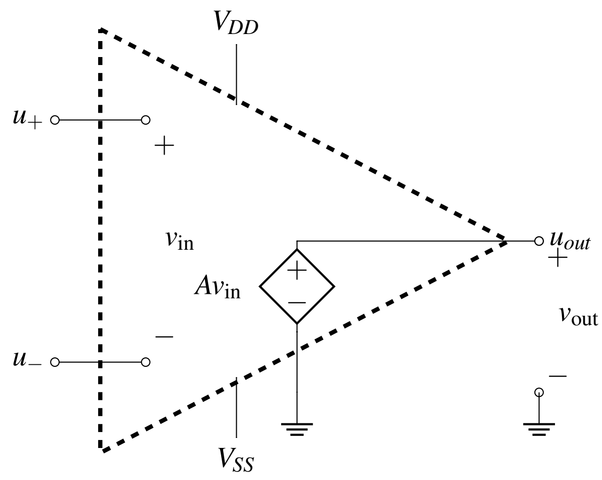


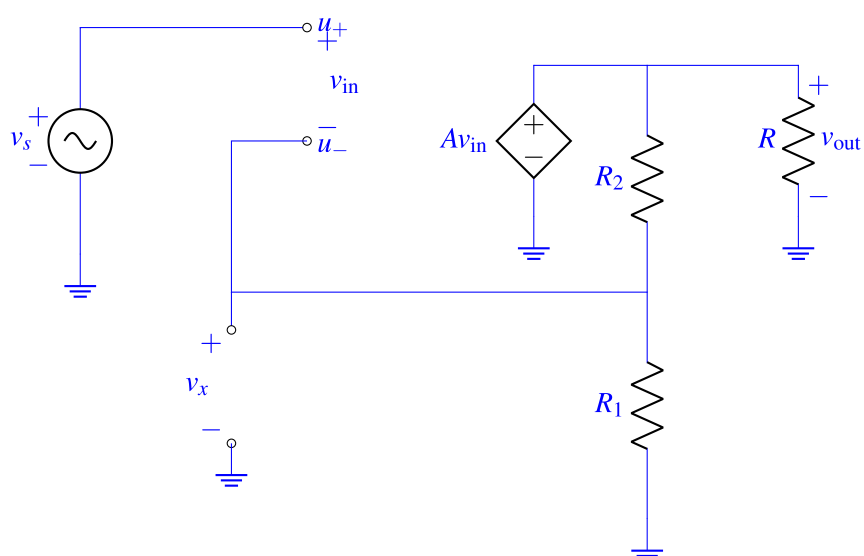
Figure 2: Op-amp model

(f) We will now examine what happens when A is not ∞. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, **by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.**

Now, using this setup, calculate v_{out} and v_x in terms of A, v_s, R_1, R_2 and R. Is the magnitude of v_x larger or smaller than the magnitude of v_s? Do these values depend on R? *Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.*

Solution:

This is the equivalent circuit of the op-amp:



Since v_{out} is connected to the output of the op-amp, which is a voltage source, we can determine v_{out}:

$$\begin{aligned} v_{\text{out}} &= A(u_+ - u_-) \\ &= A(v_s - v_x) \end{aligned}$$

Since there is no current flowing into the op-amp input terminals from nodes u_+ and u_-, R_1 and R_2 form a voltage divider and $v_x = v_{\text{out}}\left(\frac{R_1}{R_1+R_2}\right)$. Thus, substituting and solving for v_{out}:

$$v_{\text{out}} = A\left(v_s - v_{\text{out}}\frac{R_1}{R_1+R_2}\right)$$
$$v_{\text{out}} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

Knowing v_{out}, we can find v_x:

$$v_x = \frac{v_s}{1+\frac{R_1+R_2}{AR_1}}$$

Notice that v_x is slightly smaller than v_s, meaning that in equilibrium in the non-ideal case, v_+ and v_- are not equal. v_{out} and v_x do not depend on R, which means that we can treat v_{out} as a voltage source that supplies a constant voltage independent of the load R.

(g) Using your solution to the previous part, calculate the limits of v_{out} and v_x as $A \to \infty$. You should get the same answer as in part (d) for v_{out}.

Solution:

As $A \to \infty$, the fraction $\frac{1}{A} \to 0$, so

$$v_{\text{out}} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

converges to

$$v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+0}\right) = v_s\left(\frac{R_1+R_2}{R_1}\right).$$

Therefore, the limits as $A \to \infty$ are:

$$v_{\text{out}} \to v_s\left(\frac{R_1+R_2}{R_1}\right)$$
$$v_x \to v_s$$

If we observe the op-amp is in negative feedback, we can apply the fact that $u_+ = u_-$. We get $v_x = v_s$. Then the current i flowing through R_1 to ground is $\frac{v_s}{R_1}$. By KCL, this same current flows through R_2 since no current flows into the negative input terminal of the op-amp (u_-). Thus, the voltage drop across R_2 is $v_{\text{out}} - v_x = i \cdot R_2 = v_s\left(\frac{R_2}{R_1}\right)$. Therefore, $v_{\text{out}} = v_s + v_s\left(\frac{R_2}{R_1}\right) = v_s\left(\frac{R_1+R_2}{R_1}\right)$. The answers are the same if you take the limit as $A \to \infty$.

(h) **[OPTIONAL, CHALLENGE]** Now you want to make a non-inverting amplifier circuit whose gain is nominally $G_{nom} = \frac{v_{\text{out}}}{v_s} = 1 + \frac{R_2}{R_1} = 4$. However, G_{nom} can only be achieved only if the op-amp is ideal, i.e, if its internal gain $A \to \infty$. But, as with most considerations in the physical world, we must account for nonidealities! In reality, because you will be working with an op-amp with finite gain A, your designed circuit gain may come close to but will never quite reach G_{nom} as a result of the real op-amp's finite internal gain A.

Suppose you would like your real op-amp circuit to have a maximum error of 1% (i.e, a minimum circuit gain of 3.96, i.e. $\frac{v_{\text{out}}}{v_s} \geq 3.96$). Remember that only if your op-amp were ideal, you would have a nominal circuit gain of $G_{nom} = \frac{v_{\text{out}}}{v_s} = 1 + \frac{R_2}{R_1} = 4$.

What is the minimum required value of A, called A_{min}, to achieve that specification? *Hint: Use your expression of* v_{out} *in part (f) to find an expression for* $G_{min} = \frac{v_{\text{out}}}{v_s}$ *when* $A \not\to \infty$.

Solution: From the previous part, $v_{\text{out}} = v_s \left(\frac{1}{\frac{R_1}{R_1+R_2} + \frac{1}{A}} \right)$. After algebraic manipulations, we get

$$v_{out} = v_s \left(\frac{A(R_1+R_2)}{R_1+R_2+AR_1} \right)$$

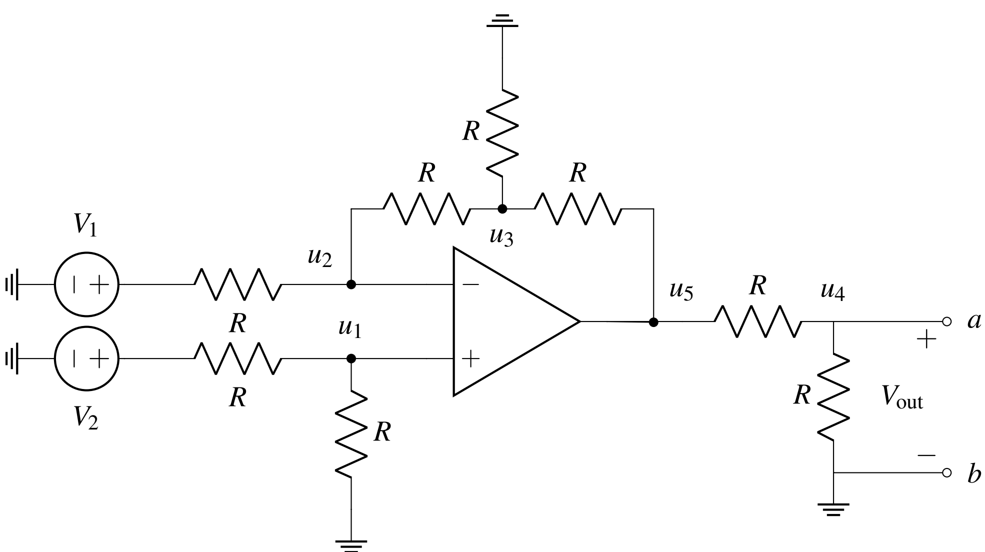
We are interested in the op-amp's minimum gain A_{min}, which gives us the circuit's corresponding minimum gain G_{min}.
We define the minimum (actual - i.e. corresponding to a non-infinite $A = A_{min}$) gain as: $G_{min} = \frac{v_{out}}{v_s}$
We also define the nominal (ideal - i.e. corresponding to an infinite A) gain as: $G_{nom} = 1 + \frac{R_2}{R_1}$.
Rewriting A_{min} in terms of G_{nom} and G_{min} gives:

$$\begin{aligned} A_{min} &= \frac{G_{min} G_{nom}}{G_{nom} - G_{min}} \\ &= 396 \end{aligned}$$

Notice that the op-amp's minimum gain is independent of the resistor values. In general, if we wanted an error of less than ε, then the following will approximately hold: $\frac{A_{min}}{G_{nom}} > \frac{1}{\varepsilon}$.

5. Op Amp Nodal Analysis

Consider this op amp circuit below. We are interested in analyzing its input-output relationship, finding the Thevenin equivalent of this op amp circuit, and making some observations about the resulting equivalent.



(a) What is the node voltage at u_1?

Solution: At node u_1, if we apply the ideal op amp assumptions, there should be no current going into the positive terminal. This means we can interpret the resistor network attached to the positive terminal as a voltage divider.

$$u_1 = \frac{R}{R+R} V_2 = \frac{V_2}{2}$$

(b) Write a KCL equation at node u_2.

Solution: At node u_2, we can write the KCL equation considering that there will be no current going into the negative terminal.

$$\frac{u_2 - V_1}{R} + \frac{u_2 - u_3}{R} = 0$$

(c) Write a KCL equation at node u_3.

Solution: At node u_3, the KCL equation is:

$$\frac{u_3 - u_2}{R} + \frac{u_3 - 0V}{R} + \frac{u_3 - u_5}{R} = 0$$

(d) Write an expression relating voltages u_4 and u_5.

Solution: At node u_5, there is a voltage divider, where u_4 is the node voltage that has the same value as the branch voltage of the resistor that bridges terminals a and b.

$$u_4 = \frac{R}{R+R} u_5 = \frac{u_5}{2}$$

Note that the output node with node voltage u_5 did not have a KCL equation written for it. This is because the output is determined by a dependent voltage source and the current coming out from the source will not be expressible until we've found all the node voltages.

(e) Noting that this circuit is in negative feedback and putting together every expression we have derived in previous parts, find an expression for V_{out} as a function of V_1 and V_2

Solution: Since the circuit is in negative feedback, the input terminal voltages should be the same: $u_1 = u_2$. Substituting into the KCL equations, we have:

$$\frac{u_1 - V_1}{R} + \frac{u_1 - u_3}{R} = 0$$

$$\frac{u_3 - u_1}{R} + \frac{u_3}{R} + \frac{u_3 - u_5}{R} = 0$$

Treating u_1 and V_1 as knowns, the first KCL equation tells us that u_3 is:

$$u_3 = 2u_1 - V_1 = V_2 - V_1$$

Treating u_3 and u_1 as knowns, the second KCL equation tells us that u_5 is:

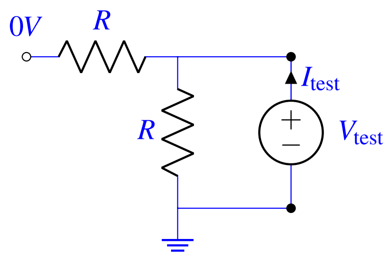
$$\begin{aligned} u_5 &= 3u_3 - u_1 \\ &= 3V_2 - 3V_1 - \frac{V_2}{2} = \frac{5}{2}V_2 - 3V_1 \end{aligned}$$

Lastly, our output voltage $u_4 = V_{\text{out}} = V_{Th}$ is:

$$u_4 = V_{\text{out}} = \frac{\frac{5}{2}V_2 - 3V_1}{2} = \frac{5}{4}V_2 - \frac{3}{2}V_1$$

(f) Turn off all independent sources ($V_1 = V_2 = 0V$). What is the equivalent resistance as seen between terminals a and b? This will be your Thevenin resistance, R_{Th}. (Hint: Consider what the voltage at the output of the op amp becomes and use a test source, or replace the op amp with its internal model where it has a dependent source.)

Solution: When both inputs V_1 and V_2 are off, the analysis in the previous subpart showed that u_5, the node voltage at the output of the op amp would be 0V. If this is the case, by applying a test source we have:



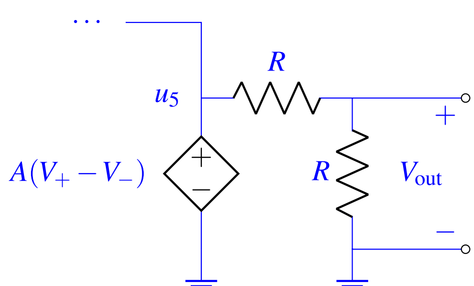
Since both resistors will have branch voltages of V_{test} over them, I_{test} can be written as:

$$I_{\text{test}} = \frac{V_{\text{test}}}{R} + \frac{V_{\text{test}}}{R} = \frac{2V_{\text{test}}}{R}$$

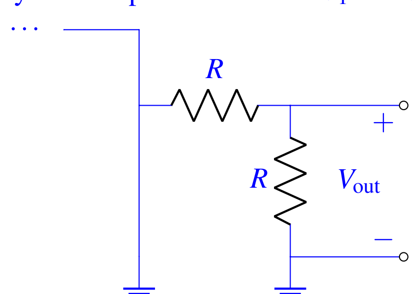
So the equivalent resistance as seen from the output (which is also the Thevenin resistance since we turned off all sources) is:

$$R_{eq} = \frac{V_{\text{test}}}{I_{\text{test}}} = \frac{R}{2}$$

Another way to approach the problem is to consider the internal model of the op amp:



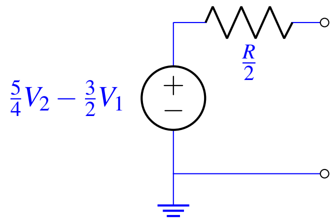
The output u_5 being zero when V_1 and V_2 are zero essentially means the dependent source is off and behaves like a short - we can turn off the dependent source in this case because it is directly influenced by the independent sources V_1 and V_2:



In this scenario, the equivalent resistance seen at the output is just $R||R = \frac{R}{2}$ since the resistors are in parallel.

(g) Use what you found in previous parts to draw the Thevenin equivalent.

Solution: The Thevenin equivalent is given by the following circuit:



(h) **Practice (Optional)**: Does the Thevenin resistance depend on all the resistors or a strict subset? What might explain this?

Solution: Since the output of an ideal op amp is a dependent voltage source, only the resistances that come after the output it will come into play, which is why we saw only the divider at the output influence the resistance.

This highlights the benefit of an op amp in allowing circuits to present with a uncomplicated or choosable Thevenin equivalent resistance (e.g. a buffer, 0 resistance) so that designed circuit modules can be connected together with predictable effect.

6. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

Solution:

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.

