EECS 16A Designing Information Devices and Systems I
Spring 2022 Homework 10

This homework is due April 8, 2022, at 23:59.
Self-grades are due April 11, 2022, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw10.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. **Reading Assignment**

   No submission is required for this problem, however we ask that you read and understand the notes.

   For this homework, please read Note 17A to learn about comparators and op-amps, and Note 17B to learn about charge sharing. You are always encouraged to read beyond this as well.

   (a) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what is the minimum/maximum value of V_{out}?

   (b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

2. **Fun With Charge Sharing**

   (a) Capacitors C_1 and C_2 are charged to V_1 and V_2 and switch S_1 is open for time $t < 0$. At time $t = 0$, switch S_1 is closed. Calculate V_1 at time $t > 0$.

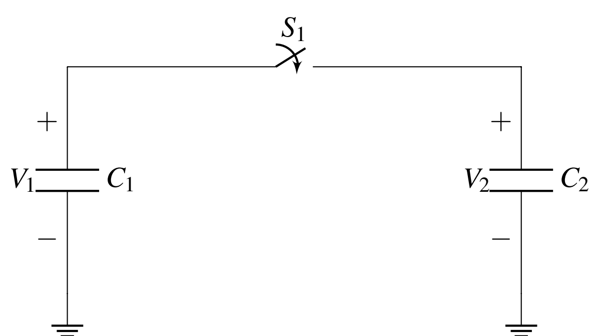
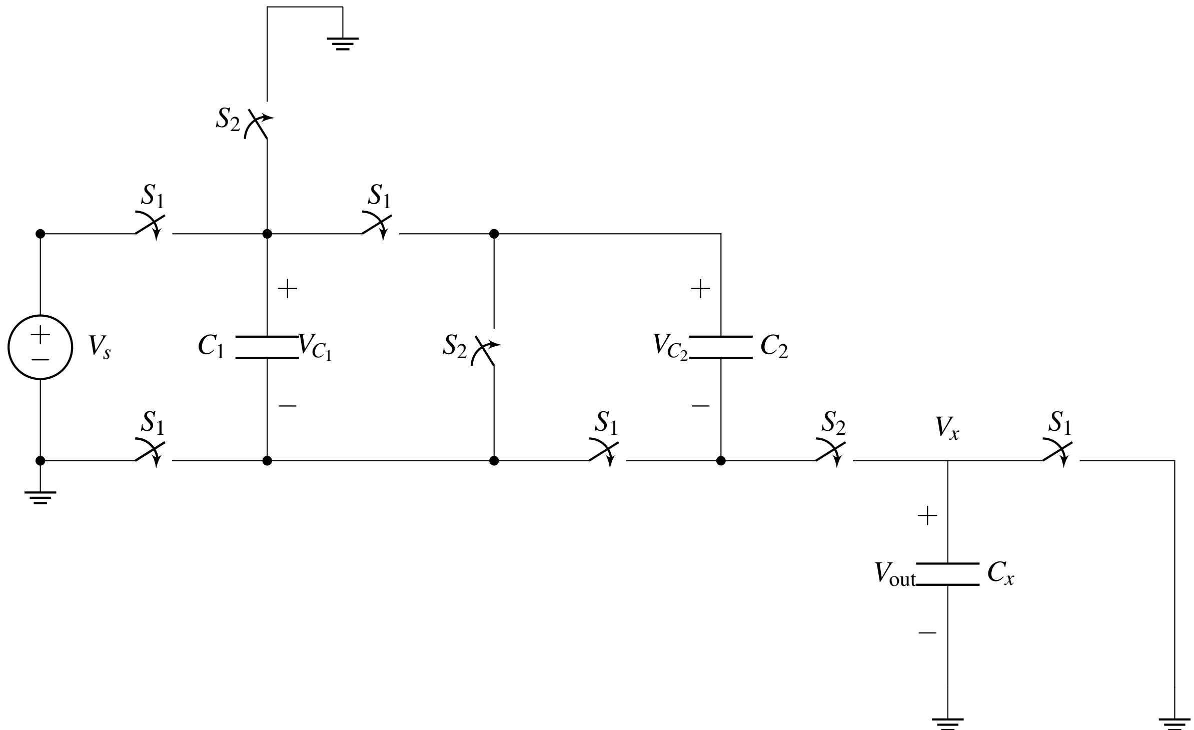


Figure 1: Capacitor Charge Sharing

   Use the following values: $C_1 = 1\text{F}$, $C_2 = 4\text{F}$, $V_1 = 6\text{V}$, $V_2 = 1\text{V}$.

(b) The circuit shown below operates in two phases. During phase 1, switches labeled S_1 are closed and switches S_2 are open. During phase 2, switches S_1 are open and switches S_2 are closed. Assume that the initial voltage on $C_x = 0$.



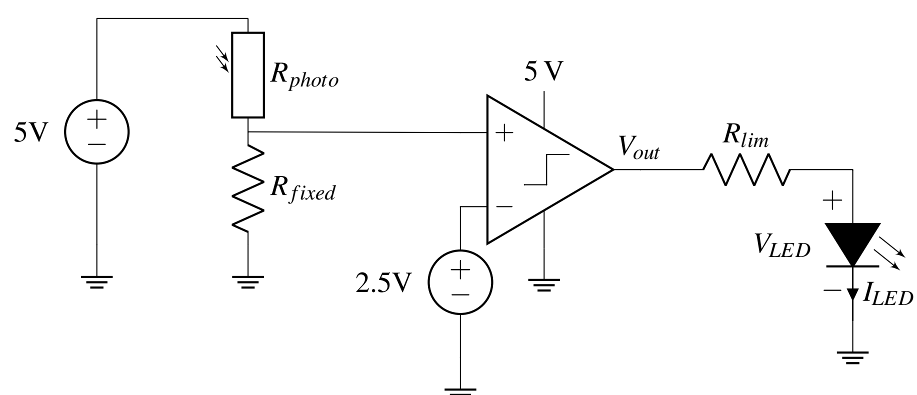
i. Redraw the circuit during phase 1. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$.

ii. Redraw the circuit during phase 2. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$.

iii. Calculate the value of the voltage V_{out} during phase 2 as a function of C_0, C_x, and V_s. Use $C_1 = C_2 = C_0$.

3. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) "alarm" if the kitchen drawer is opened.



Note R_{photo} is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

V_{LED} indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is V_+, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of R_{photo} and R_{fixed}.

(b) We now want to choose a value for R_{fixed}. From the photoresistor's datasheet, we see the resistance in "light" conditions (i.e. drawer open) is $1\,\text{k}\Omega$. In "dark" conditions (i.e. drawer closed), the resistance is $10\,\text{k}\Omega$.

To ensure the comparator detects the light condition with more tolerance, we decide to design R_{fixed} so that V_+ is $3\,\text{V}$ under the "light" condition. Solve for the value of R_{fixed} to meet this specification.

(c) Write down V_{out} with any conditions in terms of V_+. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

(d) Using your answers to the previous parts, write down V_{out} with the conditions on its output in terms of R_{photo}. You can substitute the value of R_{fixed} you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

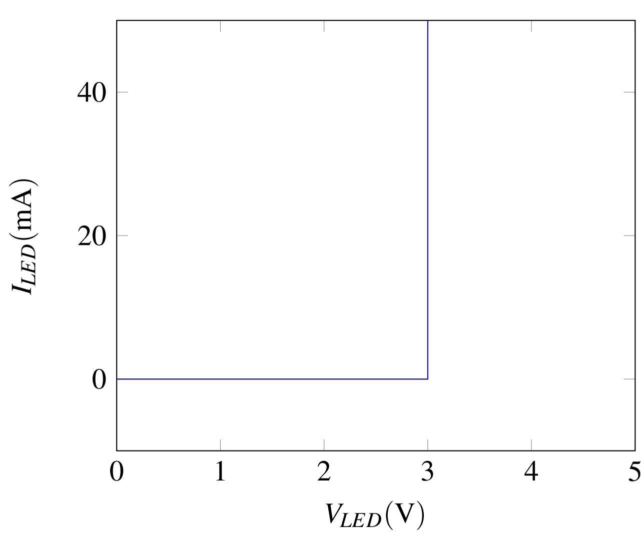
(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED's datasheet, the forward voltage, V_F is $3\,\text{V}$. Essentially, if V_{LED} is less than this voltage, the LED won't light up and I_{LED} will be $0\,\text{A}$.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

i. If the voltage across the LED is less than $V_F = 3\,\text{V}$ or if $I_{LED} < 0\,\text{A}$, then the LED acts like an open circuit.

ii. If the voltage across the LED is $V_F = 3\,\text{V}$, then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).

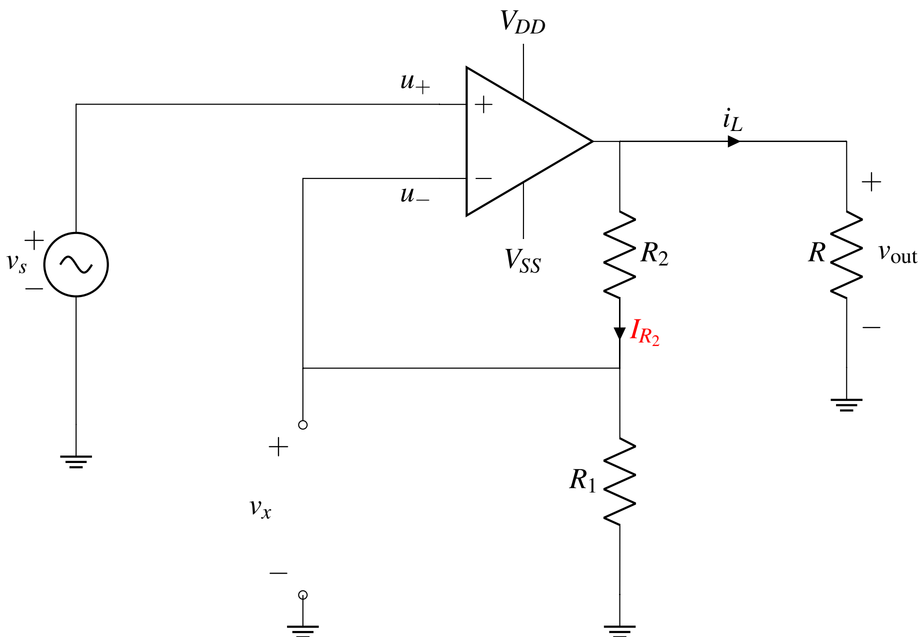


To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for I_{LED} is $20\,\text{mA}$.

Find the value of the current-limiting resistor, R_{lim}, such that when the photoresistor is in the "light" condition, $I_{LED} = 20\,\text{mA}$.

4. Op-Amp in Negative Feedback

In this question, we analyze op-amp circuits that have finite op-amp gain A. We replace the op-amp with its circuit model with parameterized gain and observe the gain's effect on terminal and output voltages as the gain approaches infinity. **Note here that $V_{SS} = -V_{DD}$.**



For parts (a) - (e) only, assume that the op-amp is ideal (i.e., $A \to \infty$). We will consider the case of finite gain A in parts (f) - (h).

(a) Consider the circuit shown above and $V_{SS} = -V_{DD}$. What is $u_+ - u_-$?

(b) Find v_x as a function of v_{out}.

(c) What is I_{R_2}, i.e. the current flowing through R_2 as a function of v_s? *Hint: Find the current through R_1 first.*

(d) Find v_{out} as a function of v_s.

(e) What is the current i_L through the load resistor R? Give your answer in terms of v_{out}.

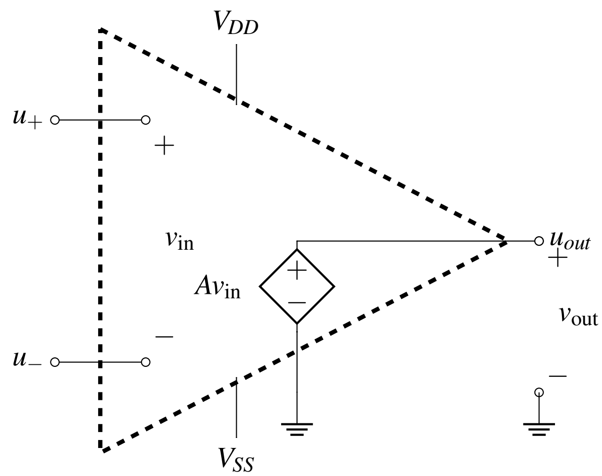


Figure 2: Op-amp model

(f) We will now examine what happens when A is not ∞. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, **by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.**

Now, using this setup, calculate v_{out} and v_x in terms of A, v_s, R_1, R_2 and R. Is the magnitude of v_x larger or smaller than the magnitude of v_s? Do these values depend on R? *Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.*

(g) Using your solution to the previous part, calculate the limits of v_{out} and v_x as $A \to \infty$. You should get the same answer as in part (d) for v_{out}.

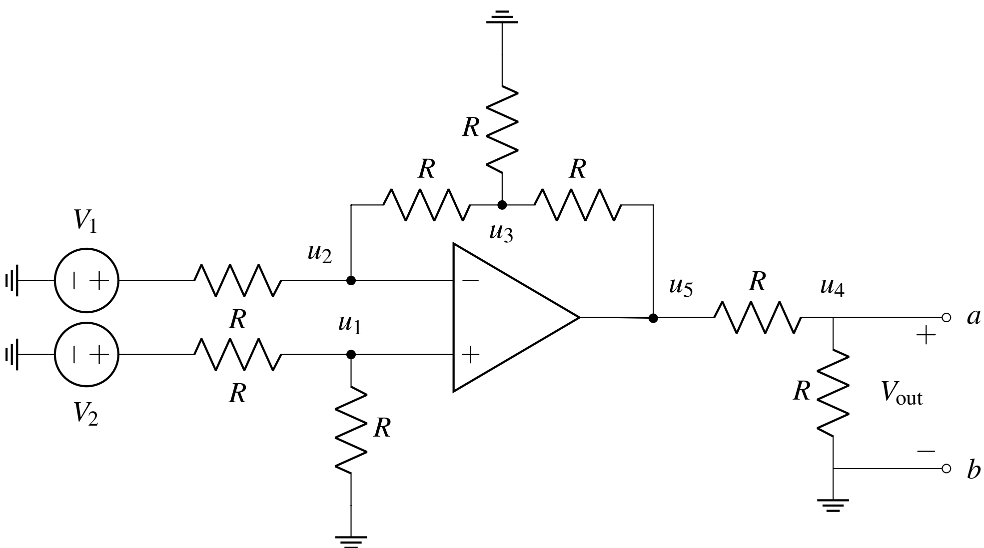
(h) **[OPTIONAL, CHALLENGE]** Now you want to make a non-inverting amplifier circuit whose gain is nominally $G_{nom} = \frac{v_{\text{out}}}{v_s} = 1 + \frac{R_2}{R_1} = 4$. However, G_{nom} can only be achieved only if the op-amp is ideal, i.e, if its internal gain $A \to \infty$. But, as with most considerations in the physical world, we must account for nonidealities! In reality, because you will be working with an op-amp with finite gain A, your designed circuit gain may come close to but will never quite reach G_{nom} as a result of the real op-amp's finite internal gain A.

Suppose you would like your real op-amp circuit to have a maximum error of 1% (i.e, a minimum circuit gain of 3.96, i.e. $\frac{v_{\text{out}}}{v_s} \geq 3.96$). Remember that only if your op-amp were ideal, you would have a nominal circuit gain of $G_{nom} = \frac{v_{\text{out}}}{v_s} = 1 + \frac{R_2}{R_1} = 4$.

What is the minimum required value of A, called A_{min}, to achieve that specification? *Hint: Use your expression of v_{out} in part (f) to find an expression for $G_{min} = \frac{v_{\text{out}}}{v_s}$ when $A \not\to \infty$.*

5. Op Amp Nodal Analysis

Consider this op amp circuit below. We are interested in analyzing its input-output relationship, finding the Thevenin equivalent of this op amp circuit, and making some observations about the resulting equivalent.



(a) What is the node voltage at u_1?

(b) Write a KCL equation at node u_2.

(c) Write a KCL equation at node u_3.

(d) Write an expression relating voltages u_4 and u_5.

(e) Noting that this circuit is in negative feedback and putting together every expression we have derived in previous parts, find an expression for V_{out} as a function of V_1 and V_2

(f) Turn off all independent sources ($V_1 = V_2 = 0V$). What is the equivalent resistance as seen between terminals a and b? This will be your Thevenin resistance, R_{Th}. (Hint: Consider what the voltage at the output of the op amp becomes and use a test source, or replace the op amp with its internal model where it has a dependent source.)

(g) Use what you found in parts b and c to draw the Thevenin equivalent.

(h) **Practice (Optional)**: Does the Thevenin resistance depend on all the resistors or a strict subset? What might explain this?

6. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.