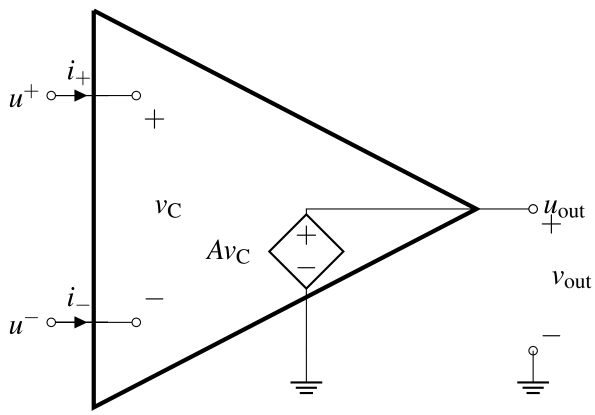
EECS 16A Spring 2022 — Designing Information Devices and Systems I — Discussion 10A

1. Op-Amp Rules

Answer: Estimated Time: 10 min

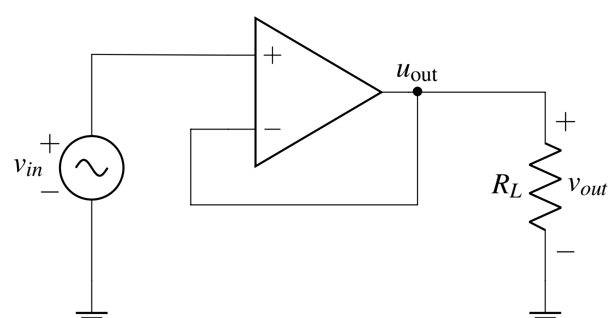
Here is an equivalent circuit of an op-amp (where we are assuming that $V_{SS} = -V_{DD}$) for reference:



(a) What are the currents flowing into the positive and negative terminals of the op-amp (i.e., what are I^+ and I^-)? Based on this answer, what are some of the advantages of using an op-amp in your circuit designs? **Answer:** The u^+ and u^- terminals have no closed circuit connection between them, and therefore no current can flow into or out of them. This is very good because we can connect an op-amp to any other circuit, and the op-amp will not disturb that circuit in any way because it does not load the circuit (it is an open circuit).

(b) Suppose we add a resistor of value R_L between u_{out} and ground. What is the value of v_{out}? Does your answer depend on R_L? In other words, how does R_L affect Av_C? What are the implications of this with respect to using op-amps in circuit design? **Answer:** Notice that u_{out} is connected directly to a controlled/dependent voltage source, and therefore v_{out} will always have to be equal to Av_C regardless of what R_L is connected to the op-amp. This is very advantageous because it means that the output of the op-amp can be connected to any other circuit (except a voltage source), and we will always get the desired/expected voltage out of the op-amp.

For the rest of the problem, consider the following op-amp circuit in negative feedback:



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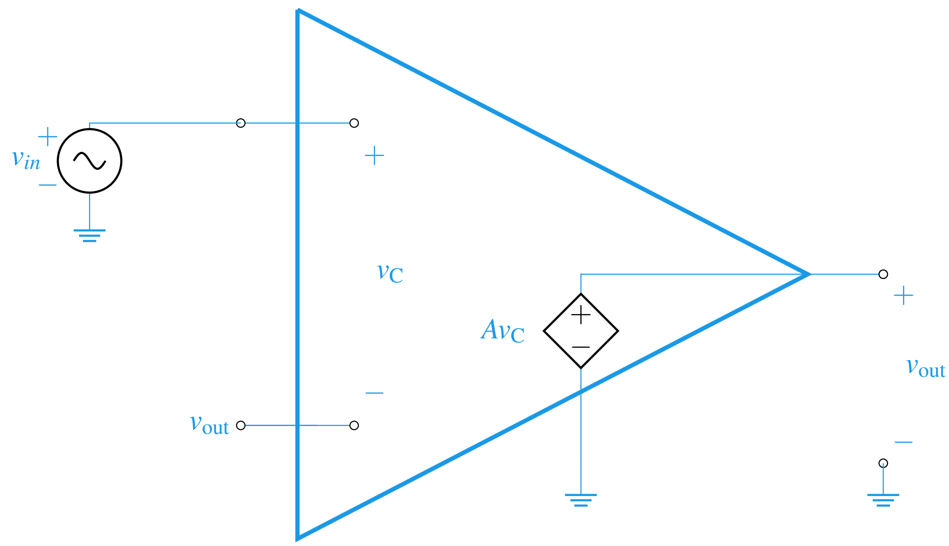
(c) Assuming that this is an ideal op-amp, what is v_{out}? **Answer:** Recall for an ideal op-amp in negative feedback, we know from the negative feedback rule that $u^+ = u^-$. In this case, $u^- = u_{\text{out}} = u^+$.

(d) Draw the equivalent circuit for this op-amp and calculate v_{out} in terms of A, v_{in}, and R_L for the circuit in negative feedback. Does v_{out} depend on R_L? What is v_{out} in the limit as $A \to \infty$? **Answer:**



Notice that the op-amp can be modeled as a voltage-controlled voltage source. Thus, we have the following equation:

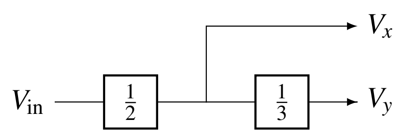
$$\begin{aligned} v_{\text{out}} &= A(v_C) \\ v_{\text{out}} &= A(v_{in} - v_{\text{out}}) \\ v_{\text{out}} + Av_{\text{out}} &= Av_{in} \\ v_{\text{out}} &= v_{in}\frac{A}{1+A} \end{aligned}$$

Thus, as $A \to \infty$, $v_{\text{out}} \to v_{\text{in}}$. This is the same as what we get after applying the op-amp rule.

Notice that output voltage does not depend on R. Thus, this circuit acts like a voltage source that provides the same voltage read at u^+ without drawing any current from the terminal at u^+. This is why the circuit is often referred to as a "unity gain buffer," "voltage follower," or just "buffer."

2. Modular Circuit Buffer

Let's try designing circuits that perform a set of mathematical operations using op-amps. While voltage dividers on their own cannot be combined without altering their behavior, op-amps can preserve their behavior when combined and thus are a perfect tool for modular circuit design. We would like to implement the block diagram shown below:



In other words, create a circuit with two outputs V_x and V_y, where $V_x = \frac{1}{2}V_{\text{in}}$ and $V_y = \frac{1}{3}V_x = \frac{1}{6}V_{\text{in}}$.

(a) Draw two voltage dividers, one for each operation (the $1/2$ and $1/3$ scalings). What relationships hold for the resistor values for the $1/2$ divider, and for the resistor values for the $1/3$ divider?

Answer: Recall our voltage divider consists of V_{in} connected to two resistors (R_1, R_2) in series with the output voltage between ground and the central node. This yields the formula

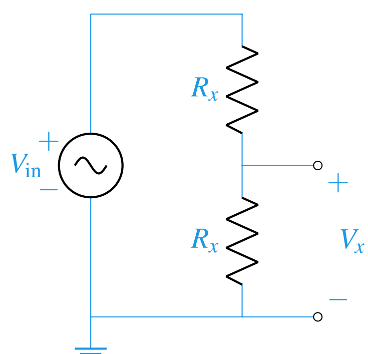
$$V_{\text{out}} = \left(\frac{R_2}{R_1 + R_2}\right) V_{\text{in}}.$$

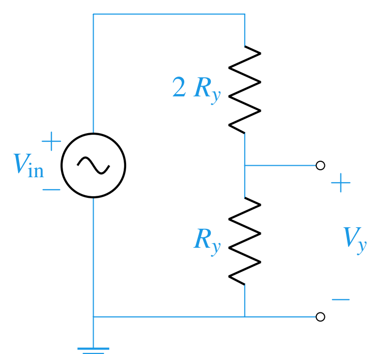
For the $1/2$ operation (V_x output) we recognize

$$\frac{1}{2} = \left(\frac{R_2}{R_1 + R_2}\right) \quad \longrightarrow \quad R_1 + R_2 = 2R_2 \quad \longrightarrow \quad R_1 = R_2 \equiv R_x.$$

For the $1/3$ operation (V_y output) we recognize

$$\frac{1}{3} = \left(\frac{R_2}{R_1 + R_2}\right) \quad \longrightarrow \quad R_1 + R_2 = 3R_2 \quad \longrightarrow \quad \frac{R_1}{2} = R_2 \equiv R_y.$$

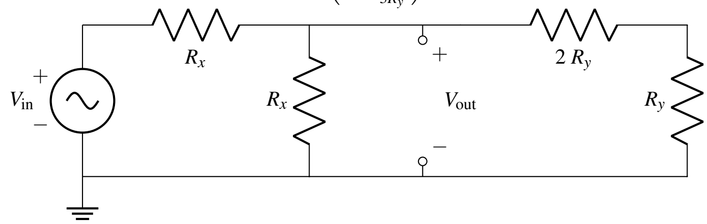




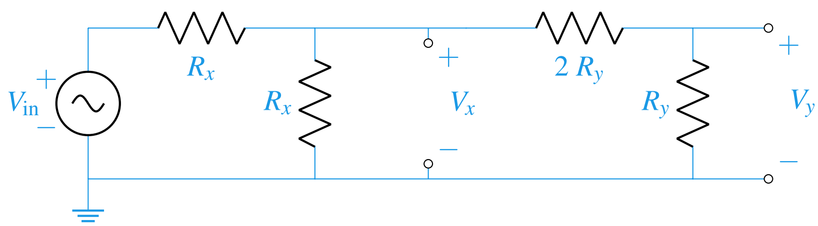
(b) If you combine the voltage dividers, made in part (a), as shown by the block diagram (output of the $1/2$ voltage divider becomes the source for the $1/3$ voltage divider circuit), do they behave as we hope (meaning $6V_{\text{in}} = 3V_x = V_y$)?

HINT: The following circuit and formula may be handy:

$$V_{\text{out}} = \left(\frac{1}{2+\frac{R_x}{3R_y}}\right)V_{\text{in}}$$



Answer: Combining the voltage divider circuits yield



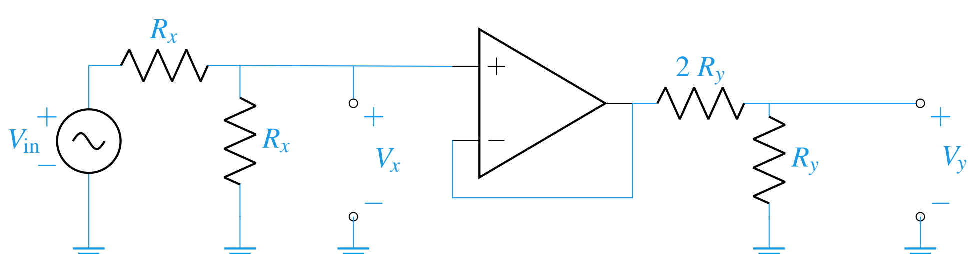
To quickly access this combined system, we may identify V_x as the result of a new equivalent voltage divider (recognizing the R_y resistors in series and that series is in parallel with R_x). The load resistor becomes $R_{eq} = \frac{3R_xR_y}{R_x+3R_y}$. This yields

$$V_x = \left(\frac{R_{eq}}{R_x+R_{eq}}\right)V_{\text{in}} = \left(\frac{1}{2+\frac{R_x}{3R_y}}\right)V_{\text{in}} \qquad V_y = \frac{1}{3}V_x = \left(\frac{1}{6+\frac{R_x}{R_y}}\right)V_{\text{in}}$$

From this stage it is evident that combining our dividers changes their behavior (although they preserve behavior in the limit $R_y >> R_x$).
The new values for V_x, V_y are dependent on values from both dividers, which means they can't be treated independently! $\square$.

(c) Perhaps we could use an op-amp (in negative-feedback) to achieve our desired behavior.
Modify the implementation you tried in part (b) using a negative feedback op-amp in order to achieve the desired V_x, V_y relations $V_x = (1/2)V_{\text{in}}$ and $V_y = (1/3)V_x = (1/6)V_{\text{in}}$.
HINT: Place the op-amp in between the dividers such that the V_x node is an input into the op-amp, while the source of the 2nd divider is the output of the op-amp!

Answer: Use the op-amp as a voltage buffer.
This means we short the op-amp's negative input to its output, since the positive input must now match its output (by the golden rules).



Since no current flows into the positive op-amp input, we've successfully isolated the dividers so they can be used in a modular fashion! □

NOTE: The V_x, V_y outputs from this configuration would change with the addition of a load on either terminal. As a follow-up, think about ways to make each output agnostic to the loads attached!