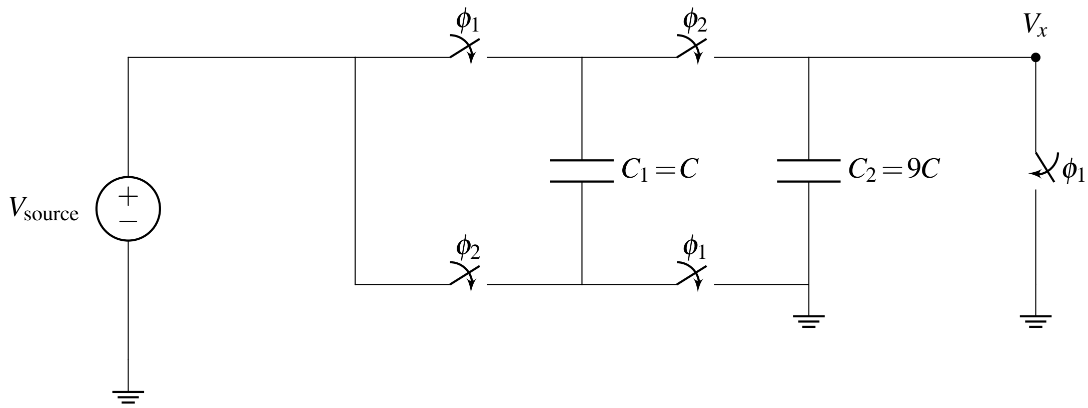
EECS 16A Designing Information Devices and Systems I
Spring 2022 Discussion 9B

1. Charge Sharing

Consider the following circuit:



In the first phase, all of the switches labeled ϕ_1 will be closed and all switches labeled ϕ_2 will be open. In the second phase, all switches labeled ϕ_1 are opened and all switches labeled ϕ_2 are closed.

(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

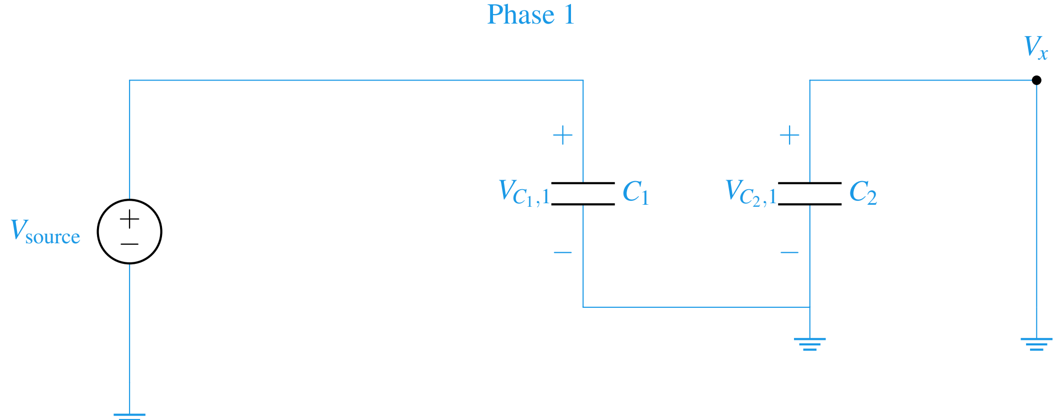
Answer:

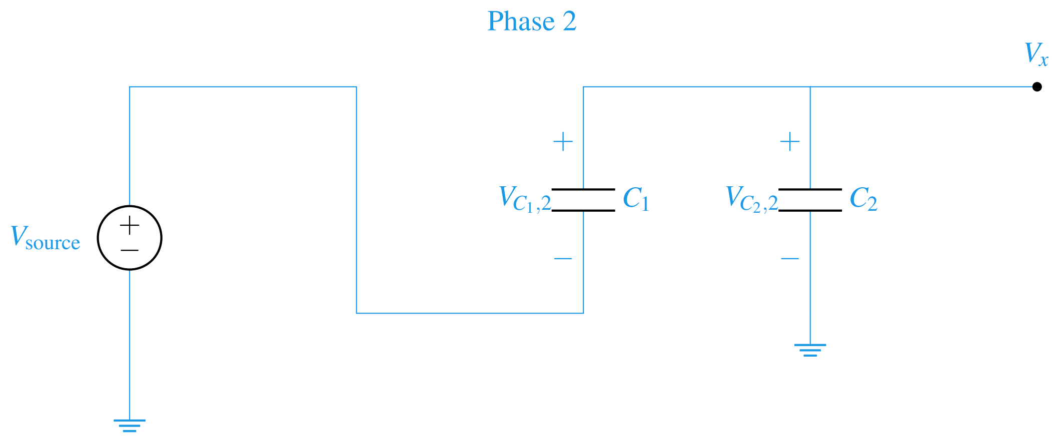
One way of marking the polarities is + on the top plate and − on the bottom plate of both C_1 and C_2. Let's call the voltage drop across C_1 V_{C_1} and across C_2 V_{C_2}.

(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

Answer:

Phase 1





In phase 1, all the switches marked as ϕ_1 are closed and switches marked as ϕ_2 are open. In phase 2, all the switches marked as ϕ_2 are closed and switches marked as ϕ_1 are open. Draw both the circuits separately, side by side, with the switches in their respective positions.

(c) Find the voltages and charges on C_1 and C_2 in phase 1. Be sure to keep the polarities of the voltages the same!

Answer:

In phase 1,

$$V_{C_1,1} = V_{\text{source}} - 0 = V_{\text{source}}$$

and

$$V_{C_2,1} = 0 - 0 = 0$$

Answer:

Next, we find the charge on each capacitor:

$$Q_{C_1,1} = V_{C_1,1}C_1 = CV_{\text{source}}$$

Note that the positive plate has a charge of $+CV_{\text{source}}$, while the negative plate has a charge of $-CV_{\text{source}}$.

$$Q_{C_2,2} = V_{C_2,1}C_2 = 0$$

(d) Now, in the second phase, find the voltage V_x.

Answer:

Where is charge conserved? To answer this, look at the top plates of C_1 and C_2. In phase 2, they are both "floating" because they are not connected to V_{source} or ground. And in phase 1, they are not connected to each other, but in phase 2, they are connected by the switch. Therefore, in phase 2, the charges on the top plates of C_1 and C_2 will be *shared*, or distributed, because they simply cannot go anywhere else. The total charge will remain the same as in phase 1. Let's find the voltages across C_1 and C_2 in phase 2 (same polarities as in phase 1!):

$$V_{C_1,2} = V_x - V_{\text{source}}$$

and

$$V_{C_2,2} = V_x$$

Now, let's find the charge stored in top plates of C_1 and C_2:

$$Q_{C_1,2} = C(V_x - V_{\text{source}})$$

and

$$Q_{C_2,2} = 9CV_x$$

Next, let's write the equation for charge conservation:

$$Q_{C_1,1} + Q_{C_2,1} = Q_{C_1,2} + Q_{C_2,2},$$

giving

$$CV_{\text{source}} + 0 = C(V_x - V_{\text{source}}) + 9CV_x,$$

which results in

$$V_x = \frac{V_{\text{source}}}{5}.$$

(e) **Practice Problem:** If the capacitor C_2 did not exist (i.e. had a capacitance of $0\,\text{F}$), what would the voltage V_x be?

Answer:

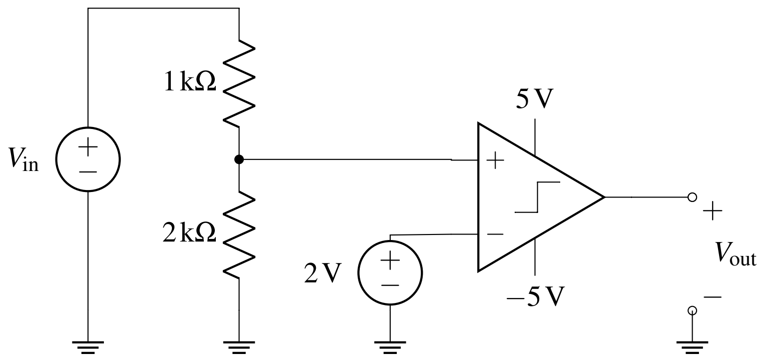
We could always go back to the equations above, plug in $C_2 = 0$, and derive $V_x = 2V_{\text{source}}$. It might be worthwhile to go over what this means for the circuit, though. If $C_2 = 0\,\text{F}$, the capacitor is actually an open circuit. (*Why?*) So we can pretend, as the question says, that C_2 does not exist. In phase 1, as before, C_1 has a voltage drop of V_{source} across it (from top to bottom) and is charged up to CV_{source}. Now, in phase 2, the top plate of C_1 is left dangling (floating). This means that the charge on the top plate of C_1 is going to be the same just like the charge on the bottom plate. We will therefore get

$$V_x = V_{\text{source}} - (-V_{\text{source}}) = 2V_{\text{source}}$$

2. Comparators

For each of the circuits shown below, plot V_{out} for V_{in} ranging from $-10\,\text{V}$ to $10\,\text{V}$ for part (a) and from $0\,\text{V}$ to $10\,\text{V}$ for part (b).

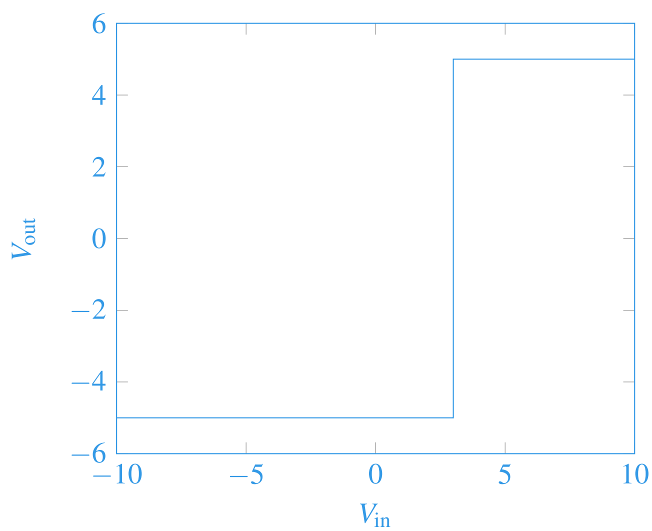
(a)



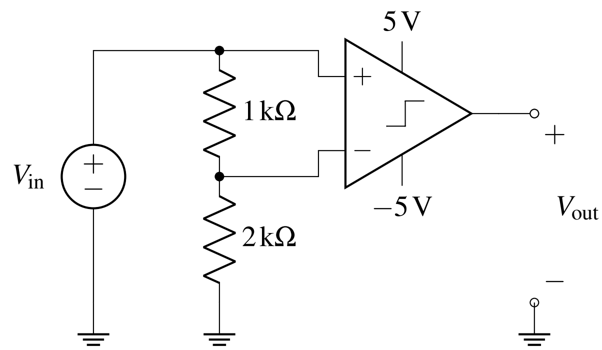
$$V_+ = \frac{2\,\text{k}\Omega}{1\,\text{k}\Omega + 2\,\text{k}\Omega} V_{in} = \frac{2}{3} V_{in}$$

$$V_- = 2\,\text{V}$$

The comparator will output positive 5V when the voltage divider's output $V_+ > 2\,\text{V}$ and thus when $V_{in} > 3\,\text{V}$. Otherwise, it will output -5V.



(b) **Practice**



When the positive terminal's voltage, V_+, is greater than the negative terminal's voltage, V_-, the output voltage would be at the positive supply rail, V_{DD}. Likewise, if the negative terminal's voltage, V_-, has a higher voltage then the value at the negative supply rail, the output voltage would be V_{SS}. Since V_- is just the output of a voltage divider with the source $V_{in} = V_+$, it will always have lower absolute value and same polarity as the positive terminal. Thus, the comparator's output will depend only on the sign of the source V_{in}.