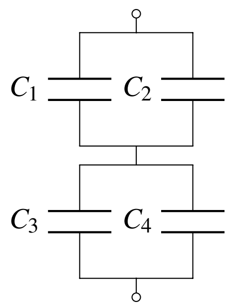
# EECS 16A Designing Information Devices and Systems I
# Spring 2022 Discussion 9A

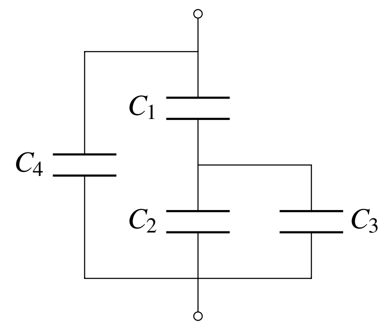
## 1. Series And Parallel Capacitors

Derive $C_{eq}$ for the following circuits.

(a)




(b)




(a) Given that we know what the relationship for capacitors in series and parallel are we can write:

$$C_{eq} = ((C_1 + C_2) \parallel (C_3 + C_4)) = \frac{(C_1 + C_2)(C_3 + C_4)}{C_1 + C_2 + C_3 + C_4}$$

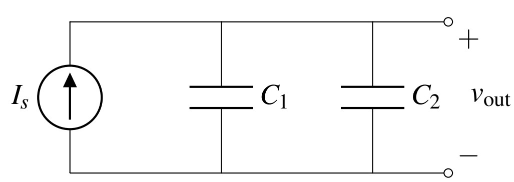
(b)

$$C_{eq} = (C_4 + (C_1 \parallel (C_2 + C_3))) = \frac{C_4(C_1 + C_2 + C_3) + C_1(C_2 + C_3)}{C_1 + C_2 + C_3}$$

## 2. Current Sources And Capacitors

(a) For the circuits given below, give an expression for $v_{\text{out}}(t)$ in terms of $I_s$, $C_1$, $C_2$, $C_3$ and $t$. Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is 0 V.

i.




**Answer:**
We can combine the two capacitors into an equivalent capacitor with capacitance $C_1 + C_2$. Again, $v_{\text{out}}(0) = 0$ because all capacitors are initially uncharged.

$$I_s = (C_1 + C_2)\frac{dv_{\text{out}}(t)}{dt}$$

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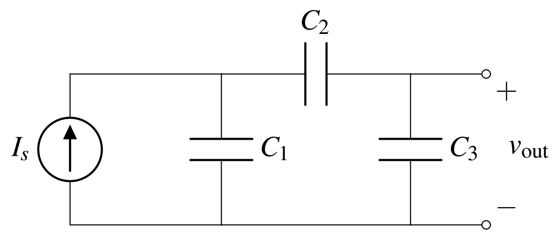
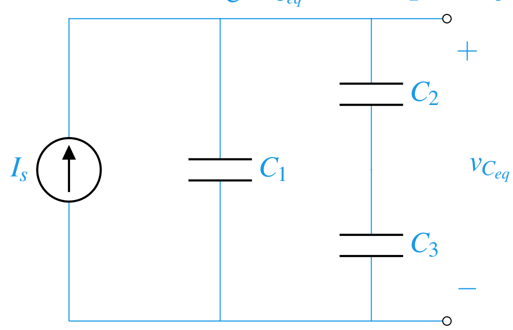
$$v_{\text{out}}(t) = \frac{I_s t}{C_1 + C_2} + v_{\text{out}}(0) = \frac{I_s t}{C_1 + C_2}$$

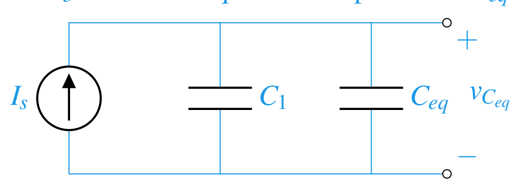
ii.




**Answer:**
Instead of finding $v_{\text{out}}$, let's first find the voltage $v_{C_{eq}}$ across $C_2$ and $C_3$.




To do this, we replace $C_2$ and $C_3$ with their equivalent capacitance $C_{eq} = C_2 \parallel C_3 = \frac{C_2 C_3}{C_2 + C_3}$.




$$v_{C_{eq}}(t) = \int \frac{I_s}{C_1 + C_{eq}} dt = \frac{I_s t}{C_1 + C_{eq}} + V_0 = \frac{I_s t}{C_1 + C_{eq}}$$

Now that we know that voltage across the equivalent capacitor $C_{eq}$, we can find the current flowing through the equivalent capacitor $C_{eq}$.

$$i_{C_{eq}}(t) = C_{eq} \frac{d v_{C_{eq}}(t)}{dt} = \frac{C_{eq} I_s}{C_1 + C_{eq}}$$

Note that the current $i_{C_{eq}}$ is equal to the current flowing through $C_3$ since $C_2$ and $C_3$ were originally connected in series.

$$i_{C_3}(t) = i_{C_{eq}}(t) = \frac{C_{eq} I_s}{C_1 + C_{eq}}$$

Since $v_{\text{out}}$ is the voltage across the capacitor $C_3$, we integrate to find $v_{\text{out}}$. Again, since all capacitors are initially uncharged, $V_0 = 0$.

$$i_{C_3}(t) = C_3 \frac{d v_{\text{out}}(t)}{dt}$$

$$v_{\text{out}}(t) = \int \frac{C_{eq} I_s}{C_3 (C_1 + C_{eq})} dt = \frac{C_{eq} I_s t}{C_3 (C_1 + C_{eq})} + V_0 = \frac{\frac{C_2 C_3}{C_2 + C_3} I_s t}{C_3 \left( C_1 + \frac{C_2 C_3}{C_2 + C_3} \right)} = \frac{C_2 I_s t}{C_1 C_2 + C_1 C_3 + C_2 C_3}$$

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(b) For the circuit in subpart (i) of part (a), assume that the direction of the current is flipped at some time $t = T$. Give an expression for $v_{\text{out}}(t)$ for $t > T$ in terms of $I_s$, $C_1$ and $C_2$. For what value of $t$ will $v_{\text{out}}(t) = 0$?

**Answer:**

for $t > T$:

$$-I_s = (C_1 + C_2)\frac{dv_{\text{out}}(t)}{dt}$$

$$v_{\text{out}}(t) = \int \frac{-I_s}{C_1 + C_2} dt = \frac{I_s t}{C_1 + C_2} + v_{\text{out}}(T)$$

We know that, $v_{\text{out}}(T) = \frac{I_s T}{C_1 + C_2}$, so $v_{\text{out}}(t) = \frac{-I_s(t-T)}{C_1 + C_2} + \frac{I_s T}{C_1 + C_2}$, for $t > T$.

In order to find the value of $t$ for which $v_{\text{out}}(t) = 0$:

$$v_{\text{out}}(t) = \frac{-I_s(t-T)}{C_1 + C_2} + \frac{I_s T}{C_1 + C_2} = 0$$

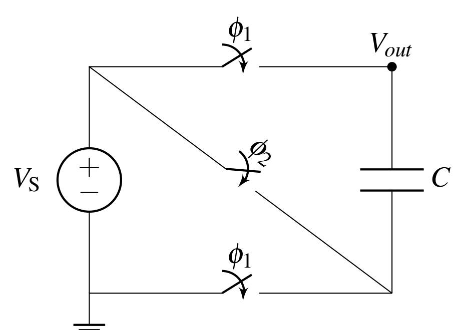
$$\frac{I_s(t-T)}{C_1 + C_2} = \frac{I_s T}{C_1 + C_2}$$

$$t - T = T$$

$$t = 2T$$

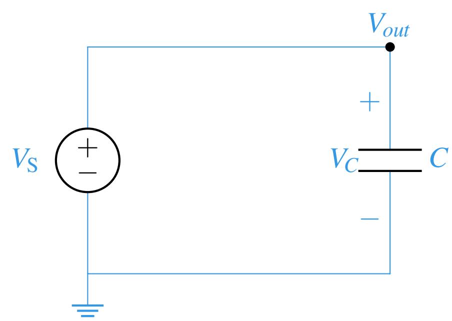
**3. Voltage Booster**

We have made extensive use of resistive voltage dividers to reduce voltage. What about a circuit that boosts voltage to a value greater than the supply $V_S = 5V$? We can do this with capacitors!



(a) In the circuit above switches $\phi_1$ are initially closed and switch $\phi_2$ is initially open. Calculate the value of the output voltage, $V_{out}$ with respect to ground, and the amount of charge stored on capacitor, $C$, at that state (phase 1).

In this setting we have the following equivalent circuit:

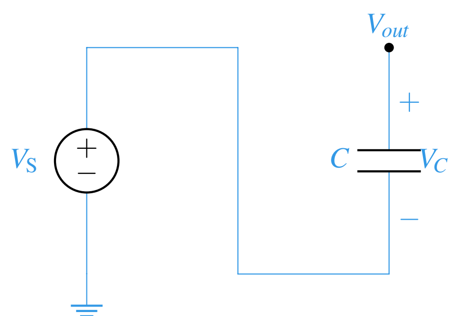



Hence,

$$V_{out} = V_S, \quad Q = CV_S.$$

(b) Now, after the capacitors are charged, switches $\phi_1$ are opened and switch $\phi_2$ is closed. Calculate the new voltage output voltage, $V_{out}$, at steady state.

Phase 2 equivalent ckt:




In phase 2 notice that the voltage source is connected to the *negative* plate of capacitor $C$, while the positive plate is left floating (since it is open). Hence, charge is going to be conserved on the top plate of $C$. However, in phase 2: $V_C^{\phi_2} = V_{out} - V_S$:

$$Q_C^{\phi_1} = Q_C^{\phi_2} \Rightarrow CV_S = C(V_{out} - V_S) \Rightarrow V_{out} = 2V_S = 10V!$$

We have created a voltage doubler!