#	Question	Answer(s)
1	that question stumped me haha	
2	if we know the equation already do we have to derive it?	live answered
3	that's because the capacitors are in parallel right?	live answered
4	what exam/worksheet is this? I joined late	This is a mix of Qs from different past exams, we'll be sharing annotated pdfs on Piazza after the review session
5	so if we picked above or below v1 and v2 the comparator would be useless right?	live answered
6	vscreen and vfinger have the same voltage right?	live answered
7	did everyone get the same MT2	order of Qs might be switched around
8	will current through elements always be 0 if there is no closed loop?	live answered
9	so no current = no voltage drop?	live answered
10	a little late, but is there no current at all when Is is off?	live answered
11	why don't we add Vs since it has a closed loop and Is is on?	live answered
12	How did you get Ib = Is again?	This is because the current doesn't branch out. From KCL, current entering node Vout = current leaving Vout, so Is = Ib
13	about the previous part, how does a voltage source work without any current flow/closed loop	live answered
14	can we use the current divider here?	live answered
15	how do we recognize part i is an incomplete loop? does the voltage source not generate current?	Current cannot flow through an incomplete loop (air cannot conduct electricity)
16	Im still a little confused on why IR is negative can we go over that again?	live answered
17	why is it -Is	live answered
18	How do you know that they are both coming in?	live answered
19	why did we decide Is = -Ir? if you drew the R's signs the opposite way wouldn't the answer become vout = IsR?	live answered
20	In our KCL, do we just ignore I-?	I- = 0 (Golden Rules of Op Amps)
21	which volatage is going into v-	live answered
22	how long is the review session going to be?	live answered
23	where is u1 in phase 1? or how did we determine it?	u1 is where the phase 2 switch closed. We determined it based on the + plates of the caps
24	why is it vmid - u out and not the other way around for C2	It has to do with us using the negative plate. If we had the + plate, we would have vout - vmid
25	so for qmid phase 1 = C1Vs - C2Vs we subtract because the bottom plate is negative? why do we add them in phase 2?	yes re: phase 1. For phase 2, the negative was absorbed into -(Vout - Vmid) = (Vmid - Vout)
26	so when we're doing q = cv for floating node plates, can we just always do the voltage of the floating node - the voltage connected to the other plate? and then we don't have to worry about + or - plates?	