# EECS 16A Designing Information Devices and Systems I
# Fall 2022 Homework 10

**This homework is due November 11, 2022, at 23:59.**
**Self-grades are due November 14, 2022, at 23:59.**

**Submission Format**
Your homework submission should consist of **one** file.

- `hw10.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

## 1. Reading Assignment

For this homework, please read Note 17A to learn about comparators and op-amps, Note 17B to learn about charge sharing, as well as the charge sharing circuit cookbook in the resources section of the course website. You are always encouraged to read beyond this as well.

(a) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what is the minimum/maximum value of $V_{out}$?

(b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

**Solution:**

a) The minimum op-amp output will always be the value of the $V_{SS}$ supply rail, and thus 0V in this case. The maximum op-amp output will always be the value of the $V_{DD}$ supply rail, and thus 5V in this case.

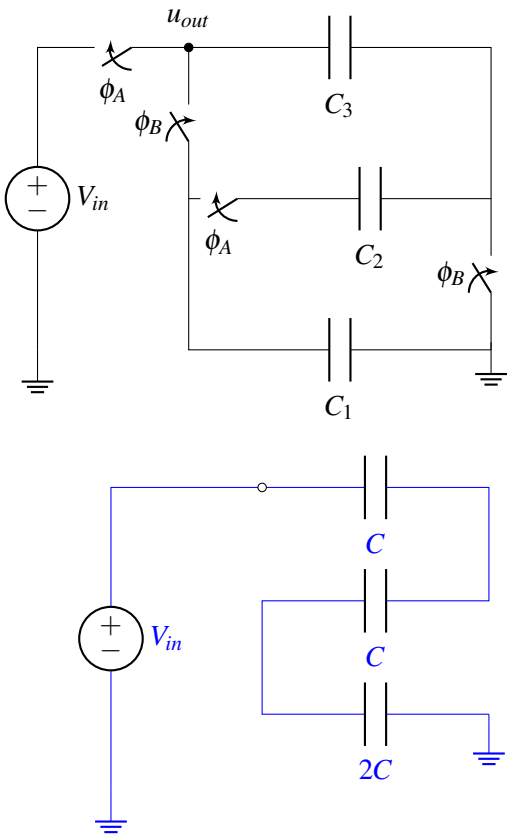
b) A comparator gives a binary output of either a high value or a low value depending on the difference of voltage between its two input terminals. Thus, comparators can be used as indicators or switches. In the case of a touchscreen, a comparator can indicate whether or not a touch occurs. This can be done by hooking up one of the comparator terminals to the equivalent capacitance of the touchscreen, and the other terminal to a reference voltage source. The value of this reference voltage source needs to be between the peak of the voltage over the capacitor with and without touch. Thus, when a touch occurs, the difference between the input terminals will invert in sign, and the comparator will respond.

## 2. Charge sharing check-in

(a) Let us analyze the capacitor circuit shown below. Let us set all of the capacitors to have the same capacitance $C_1 = 2C$ and $C_2 = C_3 = C$. Assume that all capacitors start without any initial charge, i.e. they are completely discharged before phase $A$.

The switches for phase $A$ close first and the capacitors charge up completely. Those switches are then disconnected and the switches for phase $B$ are closed. **What is the voltage at node $u_{out}$ in phase $B$ in terms of $C$ and $V_{in}$?**

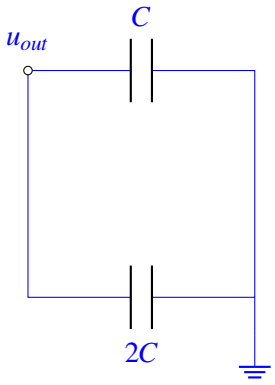
**Solution:** First we draw out the circuit in phase $A$:




We must find the equivalent capacitance for the capacitors in series: $C_{eq} = 2C/5$.

With this simplified circuit, we identify a charge of $Q_A = +\frac{2}{5}CV_{in}$ on each positive plates (and conversely $-\frac{2}{5}CV_{in}$ on the negative plates). Note that each plate must have the same charge since the capacitors are conencted in series.

Next, we draw the circuit in phase $B$:

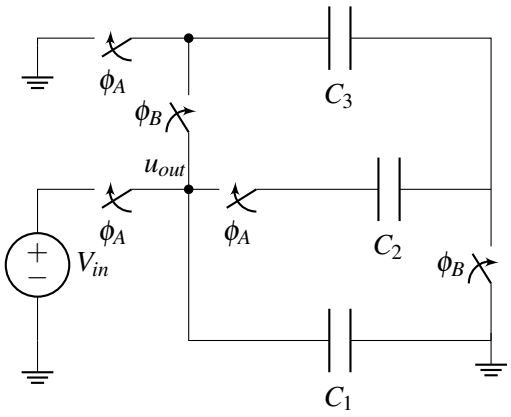



Note that since capacitor $C_2$ is not connected to node $u_{out}$ in phase $B$ we do not need to consider it here and can exclude it from our drawing. At the floating node $u_{out}$, we see the positive plates of the capacitors $C_1$ and $C_3$ are connected. The charge stored on those plates from phase $A$ is $+\frac{2}{5}CV_{in}$ and $\frac{2}{5}CV_{in}$. Summing these together, we get $Q = +\frac{4}{5}CV_{in}$. We can solve for the voltage at the floating node $u_{out}$ first by writing the charge at that node:

$$Q = C_{eq} \cdot u_{out}$$
$$Q = 3C \cdot u_{out}$$
$$+\frac{4}{5}CV_{in} = 3C \cdot u_{out}$$

Thus, $u_{out} = \frac{4}{15}V_{in}$.

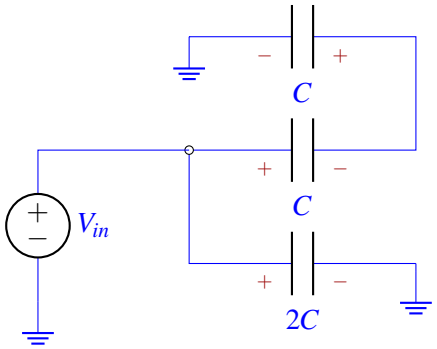
(b) Now consider the following circuit. Let us again set all of the capacitors to have the same capacitance $C_1 = 2C$ and $C_2 = C_3 = C$. Assume that all capacitors start without any initial charge, i.e. they are completely discharged before phase $A$. The switches for phase $A$ close first and the capacitors charge up completely. Those switches are then disconnected and the switches for phase $B$ are closed.




**What is the voltage at $u_{out}$ in phase B in terms of $C$ and $V_{in}$?**

**Solution:**

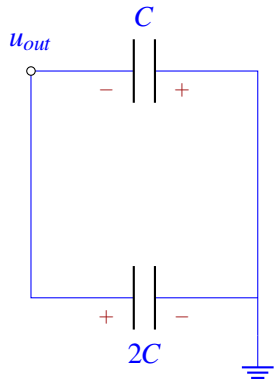
First we draw the circuit in phase $A$:




To find the charges on the top plates, we can first find the equivalent capacitance of the top two capacitors, ($C_2$ and $C_3$) in series, which is $\frac{C}{2}$.

Thus, the charge stored on the top two capacitors in phase $A$ is $\frac{1}{2}CV_{in}$. And the charge stored on the bottom capacitor is $2C \cdot V_{in}$.

Next we draw the circuit in phase $B$.



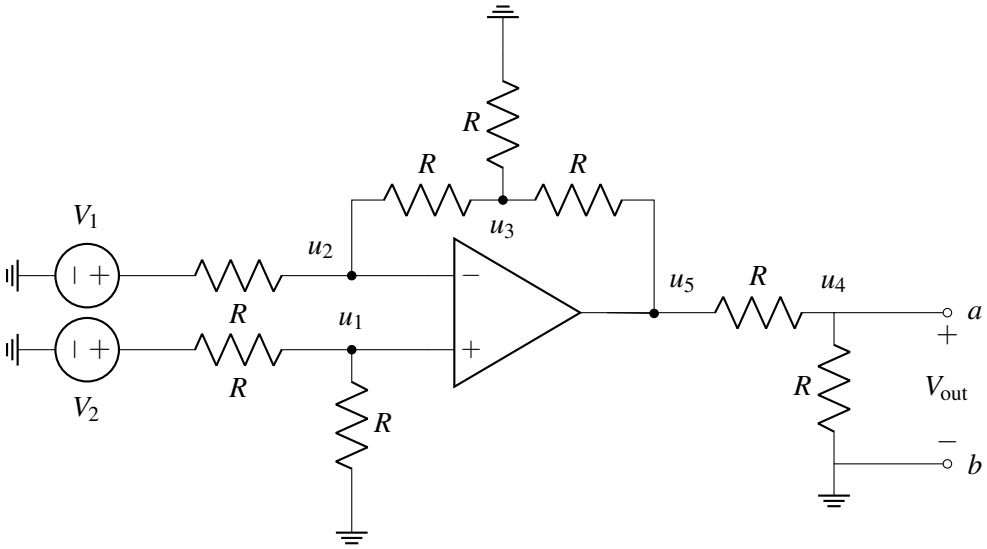

At the floating node $u_{out}$, we see the positive plate of the bottom capacitor and the *negative* plate of top capacitor are connected. Note that the polarity (positive and negative designation) is given in phase $A$ when the capacitors are being charged. These charges are $2C \cdot V_{in}$ for the bottom plate and $-\frac{C}{2}V_{in}$ for the top plate. Summed together, the charge on the floating node in phase $B$ is $Q = \frac{3}{2}CV_{in}$. Now we can find the voltage at $u_{out}$.

$$Q = C_{eq} \cdot u_{out} \quad Q = 3C \cdot u_{out}$$
$$\frac{3}{2}CV_{in} = 3C \cdot u_{out}$$

Thus, the charge at $u_{out}$ in phase $B$ is $\frac{1}{2}V_{in}$.

## 3. Op Amp Nodal Analysis

Consider this op amp circuit below. We are interested in analyzing its input-output relationship, finding the Thévenin equivalent of this op amp circuit, and making some observations about the resulting equivalent.




(a) What is the node voltage at $u_1$?

**Solution:** At node $u_1$, if we apply the ideal op amp assumptions, there should be no current going into the positive terminal. This means we can interpret the resistor network attached to the positive terminal as a voltage divider.

$$u_1 = \frac{R}{R+R}V_2 = \frac{V_2}{2}$$

(b) Write a KCL equation at node $u_2$ in terms of the node potentials $u_i$.

**Solution:** At node $u_2$, we can write the KCL equation considering that there will be no current going into the negative terminal.

$$\frac{u_2 - V_1}{R} + \frac{u_2 - u_3}{R} = 0$$

(c) Write a KCL equation at node $u_3$ in terms of the node potentials $u_i$.

**Solution:** At node $u_3$, the KCL equation is:

$$\frac{u_3 - u_2}{R} + \frac{u_3 - 0V}{R} + \frac{u_3 - u_5}{R} = 0$$

(d) Write an expression for $u_4$ in terms of $u_5$ using circuit topologies you learned in class.

**Solution:** At node $u_5$, there is a voltage divider, where $u_4$ is the node voltage that has the same value as the branch voltage of the resistor that bridges terminals $a$ and $b$.

$$u_4 = \frac{R}{R+R}u_5 = \frac{u_5}{2}$$

Note that we did not write the KCL equation for the node voltage $u_5$. This is because the output is determined by a dependent voltage source and the current coming out from the source will not be expressible until we've found all the node voltages.

(e) Noting that this circuit is in negative feedback and putting together every expression we have derived in previous parts, find an expression for $V_{out}$ as a function of $V_1$ and $V_2$.

**Solution:** Since the circuit is in negative feedback, the input terminal voltages should be the same: $u_1 = u_2$. Substituting into the KCL equations, we have:

$$\frac{u_1 - V_1}{R} + \frac{u_1 - u_3}{R} = 0$$

$$\frac{u_3 - u_1}{R} + \frac{u_3}{R} + \frac{u_3 - u_5}{R} = 0$$

Treating $u_1$ and $V_1$ as knowns, the first KCL equation tells us that $u_3$ is:

$$u_3 = 2u_1 - V_1 = V_2 - V_1$$

Treating $u_3$ and $u_1$ as knowns, the second KCL equation tells us that $u_5$ is:

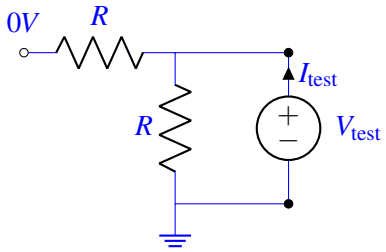
$$\begin{aligned} u_5 &= 3u_3 - u_1 \\ &= 3V_2 - 3V_1 - \frac{V_2}{2} = \frac{5}{2}V_2 - 3V_1 \end{aligned}$$

Lastly, our output voltage $u_4 = V_{\text{out}}$ is:

$$u_4 = V_{\text{out}} = \frac{\frac{5}{2}V_2 - 3V_1}{2} = \frac{5}{4}V_2 - \frac{3}{2}V_1$$

(f) Turn off all independent sources ($V_1 = V_2 = 0V$). What is the equivalent resistance as seen between terminals $a$ and $b$? This will be your Thevenin resistance, $R_{Th}$. (Hint: Consider what the voltage at the output of the op amp becomes and use a test source, or replace the op amp with its internal model where it has a dependent source.)

**Solution:** When both inputs $V_1$ and $V_2$ are off, the analysis in the previous subpart showed that $u_5$, the node voltage at the output of the op amp would be 0V. If this is the case, by applying a test source we have:



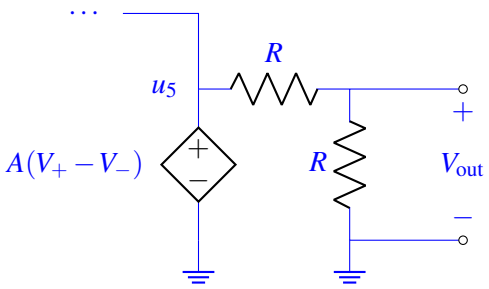

Since both resistors will have branch voltages of $V_{\text{test}}$ over them, $I_{\text{test}}$ can be written as:

$$I_{\text{test}} = \frac{V_{\text{test}}}{R} + \frac{V_{\text{test}}}{R} = \frac{2V_{\text{test}}}{R}$$

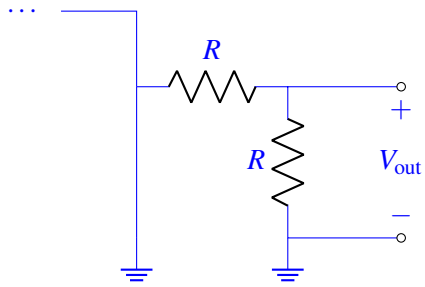
So the equivalent resistance as seen from the output (which is also the Thevenin resistance since we turned off all sources) is:

$$R_{eq} = \frac{V_{\text{test}}}{I_{\text{test}}} = \frac{R}{2}$$

Another way to approach the problem is to consider the internal model of the op amp:



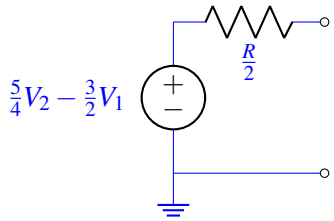

The output $u_5$ being zero when $V_1$ and $V_2$ are zero essentially means the dependent source is off and behaves like a short - we can turn off the dependent source in this case because it is directly influenced by the independent sources $V_1$ and $V_2$:




In this scenario, the equivalent resistance seen at the output is just $R||R = \frac{R}{2}$ since the resistors are in parallel.

(g) Use what you found in previous parts to draw the Thévenin equivalent.

**Solution:** The Thévenin equivalent is given by the following circuit:



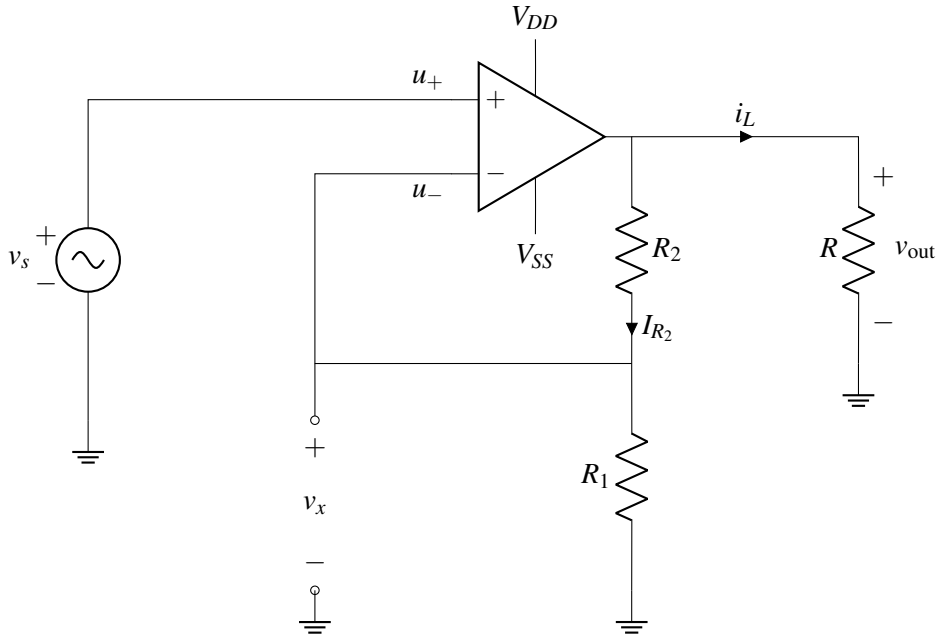

(h) **Practice (Optional)**: Does the Thévenin resistance depend on all the resistors or a strict subset? What might explain this?

**Solution:** Since the output of an ideal op amp is a dependent voltage source, only the resistances that come after the output will come into play, which is why we saw only the divider at the output influence the resistance.

This highlights the benefit of an op amp in allowing circuits to present with a uncomplicated or choosable Thévenin equivalent resistance (e.g. a buffer, 0 resistance) so that designed circuit modules can be connected together with predictable effect.

## 4. Op-Amp in Negative Feedback

In this question, we analyze op-amp circuits that have finite op-amp gain $A$. We replace the op-amp with its circuit model with parameterized gain and observe the gain's effect on the terminal and output voltages as the gain approaches infinity. **Note here that $V_{SS} = -V_{DD}$.**




**For parts (a) - (e) only, assume that the op-amp is ideal (i.e., $A \to \infty$).** We will consider the case of finite gain $A$ in parts (f) - (h).

(a) Consider the circuit shown above and $V_{SS} = -V_{DD}$. What is $u_+ - u_-$?

**Solution:** For ideal op-amp circuits in negative feedback, the voltage at the two terminals must be equal, so $u_+ - u_- = 0$.

(b) Find $v_x$ as a function of $v_{out}$.

**Solution:** We see that $v_x$ is the middle node of a voltage divider, so $v_x = v_{out}\frac{R_1}{R_1+R_2}$.

(c) What is $I_{R_2}$, i.e. the current flowing through $R_2$ as a function of $v_s$? *Hint: Find the current through $R_1$ first.*

**Solution:** The current flowing through $R_2$ is equal to the current flowing through $R_1$ since there cannot be current flowing into the op amp input. The current flowing through $R_1$ is $I_{R_1} = I_{R_2} = \frac{v_x}{R_1}$. We know from part (a) that $u_+ = u_-$, which means $v_x = v_s$. Finally, we can write $I_{R_2} = \frac{v_s}{R_1}$.

(d) Find $v_{out}$ as a function of $v_s$.

**Solution:** $v_{out} = v_{R_1} + v_P R_2 = v_s + I_{R_2} R_2$. Using the expressions for $I_{R_2}$ from part(c), $v_{out} = v_s + \frac{v_s}{R_1} R_2 = v_s \left(\frac{R_1+R_2}{R_1}\right)$. Note that $v_{out}$ could have also been found using the voltage divider equation.

(e) What is the current $i_L$ through the load resistor $R$? Give your answer in terms of $v_{out}$.

**Solution:** Using Ohm's Law, the current $i_L$ through the load is $\frac{v_{out}}{R}$.

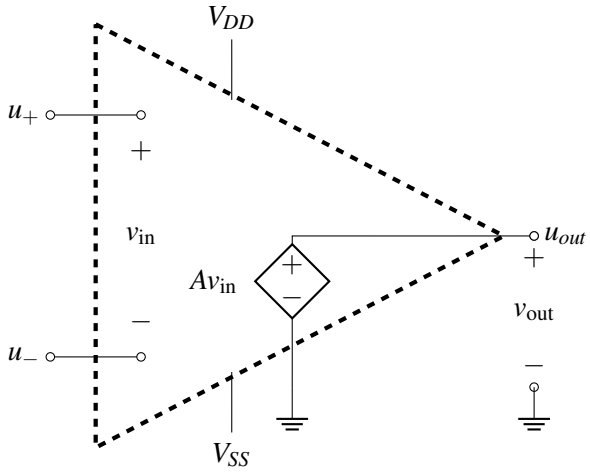


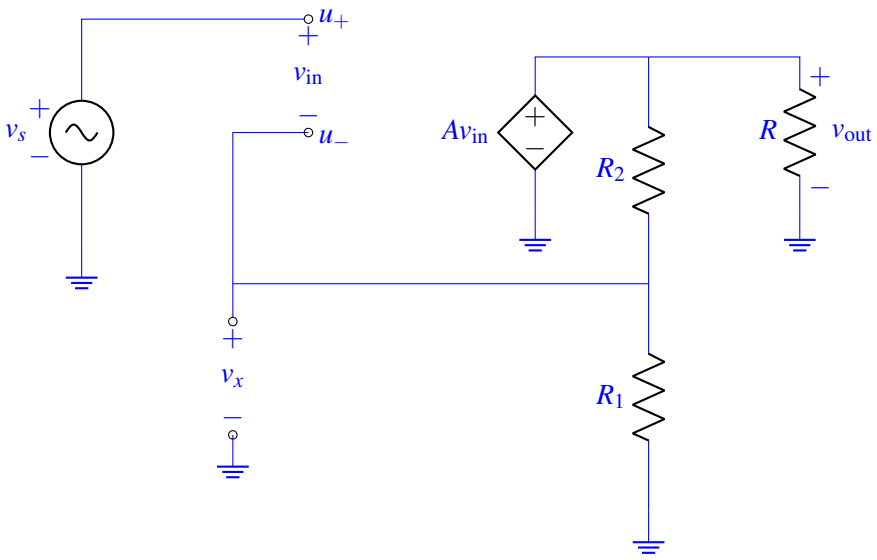

Figure 1: Op-amp model

(f) We will now examine what happens when $A$ is not $\infty$. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, **by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.**

Now, using this setup, calculate $v_{\text{out}}$ and $v_x$ in terms of $A$, $v_s$, $R_1$, $R_2$, and $R$. Is the magnitude of $v_x$ larger or smaller than the magnitude of $v_s$? Do these values depend on $R$? *Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.*

**Solution:**

This is the equivalent circuit of the op-amp:




Since $v_{out}$ is connected to the output of the op-amp, which is a voltage source, we can determine $v_{out}$:

$$\begin{aligned} v_{out} &= A(u_+ - u_-) \\ &= A(v_s - v_x) \end{aligned}$$

Since there is no current flowing into the op-amp input terminals from nodes $u_+$ and $u_-$, $R_1$ and $R_2$ form a voltage divider and $v_x = v_{out}\left(\frac{R_1}{R_1+R_2}\right)$. Thus, substituting and solving for $v_{out}$:

$$v_{out} = A\left(v_s - v_{out}\frac{R_1}{R_1+R_2}\right)$$

$$v_{out} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

Knowing $v_{out}$, we can find $v_x$:

$$v_x = \frac{v_s}{1+\frac{R_1+R_2}{AR_1}}$$

Notice that $v_x$ is slightly smaller than $v_s$, meaning that in equilibrium in the non-ideal case, $v_+$ and $v_-$ are not equal. $v_{out}$ and $v_x$ do not depend on $R$, which means that we can treat $v_{out}$ as a voltage source that supplies a constant voltage independent of the load $R$.

(g) Using your solution to the previous part, calculate the limits of $v_{out}$ and $v_x$ as $A \to \infty$. You should get the same answer as in part (d) for $v_{out}$.

**Solution:**

As $A \to \infty$, the fraction $\frac{1}{A} \to 0$, so

$$v_{out} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

converges to

$$v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+0}\right) = v_s\left(\frac{R_1+R_2}{R_1}\right).$$

Therefore, the limits as $A \to \infty$ are:

$$v_{\text{out}} \to v_s \left( \frac{R_1 + R_2}{R_1} \right)$$
$$v_x \to v_s$$

If we observe the op-amp is in negative feedback, we can apply the fact that $u_+ = u_-$. We get $v_x = v_s$. Then the current $i$ flowing through $R_1$ to ground is $\frac{v_s}{R_1}$. By KCL, this same current flows through $R_2$ since no current flows into the negative input terminal of the op-amp ($u_-$). Thus, the voltage drop across $R_2$ is $v_{\text{out}} - v_x = i \cdot R_2 = v_s \left( \frac{R_2}{R_1} \right)$. Therefore, $v_{\text{out}} = v_s + v_s \left( \frac{R_2}{R_1} \right) = v_s \left( \frac{R_1 + R_2}{R_1} \right)$. The answers are the same if you take the limit as $A \to \infty$.

## 5. Transresistance Amplifier

A common use of an op-amp is to convert a current signal into a voltage signal. This configuration is called a *transresistance amplifier*, as shown in Figure 2. (Note: In the real world, we call this a trans*impedance* amplifier. Impedance is just a fancy word to describe resistance as a function of frequency.) Assume that $V_{SS} = -V_{DD}$ for all the parts of this problem.

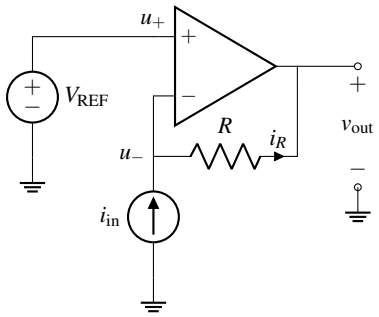



Figure 2: Transresistance amplifier

(a) What is the value of the current $i_R$ in Figure 2? *Hint: Your answer should be in terms of $i_{in}$.*

**Solution:** By the Golden Rules, since there is no current flowing into the negative terminal of the op-amp, all the current from the current source flows through the feedback resistor. Therefore, $i_R = i_{\text{in}}$.

(b) What is the voltage at the negative terminal of the op-amp $u_-$ in terms of $V_{\text{REF}}$.

**Solution:** Note that this op-amp is in negative feedback. Therefore, by the Golden Rules, the voltages at the negative and positive terminals of the op-amp are equal. Thus, the voltage at the negative terminal of the op-amp is $V_{\text{REF}}$.

(c) Using the results from parts (a) and (b), find an expression for $v_{\text{out}}$ in terms of $V_{\text{REF}}$ and $i_{\text{in}}$.

**Solution:** We can write a single KCL equation at the negative input terminal of the op-amp as follows:

$$i_{\text{in}} = \frac{V_{\text{REF}} - v_{\text{out}}}{R}$$
$$\implies v_{\text{out}} = V_{\text{REF}} - i_{\text{in}} R$$

(d) If we set $V_{\text{REF}} = 0\,\text{V}$, calculate the gain of the overall circuit $G = \frac{v_{\text{out}}}{i_{\text{in}}}$.

**Solution:** Note that in this configuration, the input signal is current $i_{in}$ (*aside: contrast this with other op-amp circuit examples that you have seen in which the input is typically a voltage*), and the output signal is voltage $v_{\text{out}}$. Therefore, in this case, you will want to report the gain of this circuit as $\frac{v_{\text{out}}}{i_{\text{in}}}$.

$$\text{Gain} = \frac{v_{\text{out}}}{i_{\text{in}}} = \frac{-i_{\text{in}}R}{i_{\text{in}}} = -R$$

## 6. Pre-Lab Questions

These questions pertain to the Pre-Lab reading for the Touch 3B lab. You can find the reading under the Touch 3B Lab section on the 'Schedule' page of the website.

(a) Why can't we have an ideal current source?

**Solution:** We need an infinite parallel resistance across the ends of a current source for it to be ideal. An infinite resistance is impossible and thus, an ideal current source is not possible to create in the real world.

(b) For the integrator circuit, if $V_{in}(t)$ is a triangle wave, what kind of wave will $I_{in}(t)$ be?

**Solution:** Triangle wave.

(c) Does $V_{out}$ increase or decrease when you touch the touchscreen?

**Solution:** $C_{pixel}$ increases with touch so $V_{out}$ will decrease since $V_{out}(t) = -\frac{1}{R_{in}C_{pixel}}\int_{t_0}^{t} V_{in}(t)\mathrm{d}t$

## 7. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

**Solution:**

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.