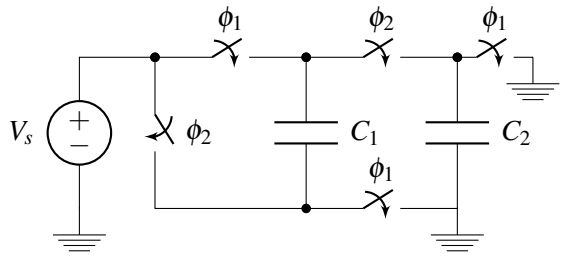
EECS 16A Designing Information Devices and Systems I Summer 2020 Note 17B

This handout outlines a detailed algorithmic procedure that solves two-phase switch capacitor circuit problems.

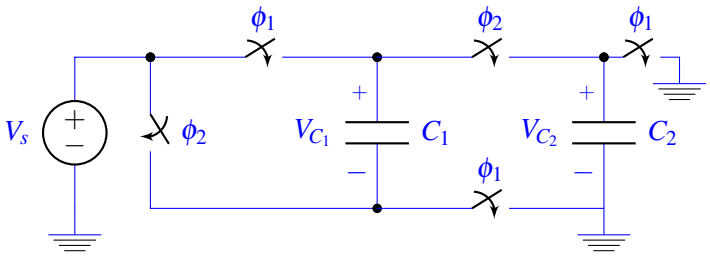
Goal: Find the voltage of all floating nodes in a 2-phase switched capacitor circuit at the end of phase 2.
Main Principle: Charge Conservation
Useful Definition: A **floating node** is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, or, as you'll see later in the course, opamp inputs or comparator inputs.

We present this algorithm by applying it to two examples, one simpler and one slightly more tricky. Note, that this method can be extended to circuits with more than 2 phases.

1. **For the switch capacitor circuit below, calculate the value of all node voltages at the end phase 2, as a function of the voltage source V_s and the capacitors C_1, C_2.**

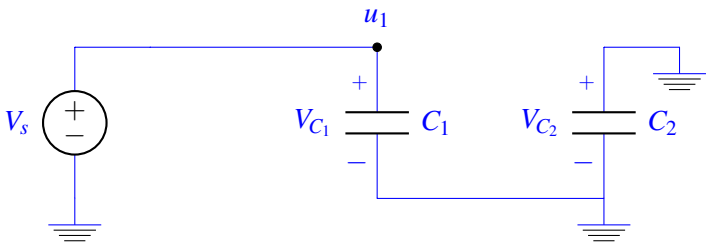


Step 1: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "−" sign. Just make sure you stay consistent with this polarity across phases.

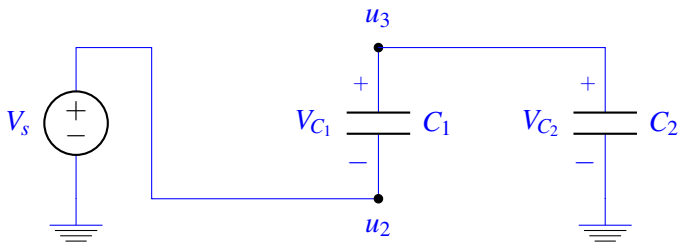


Step 2: Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the phase 1 circuit might be merged or split in phase 2.

Phase 1:



Phase 2:



Step 3: Identify all "floating" nodes in your circuit during phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.

In this case the only node that is floating during phase 2 is node u_3. (Node u_2 is connected to the voltage source, i.e. $u_2 = V_s$, and the 3^{rd} node is the ground node).

Step 4: For steps 4-6 we will **examine each phase 2 floating node individually**. Pick a floating node from the ones you found in step 3 and identify all capacitor plates connected to that node during phase 2. Then, calculate the charge on each of these plates during phase 1.
To do so, identify all nodes in your circuit during phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (step 2 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage *across* a capacitor).
Careful: The plate marked with the "$-$" sign will have $Q = -CV_C$ and the plate marked with the "$+$" sign will have $Q = CV_C$ stored onto them.
Careful 2: We assume here that you know all node voltages during phase 1. If you don't, before starting this procedure calculate the node voltages you need using one of the previously introduced circuit analysis techniques (most likely KVL will do the job).

Looking at our single floating node we can see that the "+" plates of C_1 and C_2 are connected to it during phase 2. Let's calculate the charge on these plates during **phase** ϕ_1.

$$\begin{aligned} Q_{u_3}^{\phi_1} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (V_s - 0)C_1 + 0 \\ &= V_sC_1 \end{aligned}$$

Step 5: Find the total charge on each of the floating nodes during phase 2 as a function of node voltages. Use the same process as in Step 4, but this time using the node voltages during phase 2 to write the voltages

across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

$$\begin{aligned} Q_{u_3}^{\phi_2} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (u_3 - u_2)C_1 + (u_3 - 0)C_2 \\ &= (u_3 - V_s)C_1 + u_3C_2 \end{aligned}$$

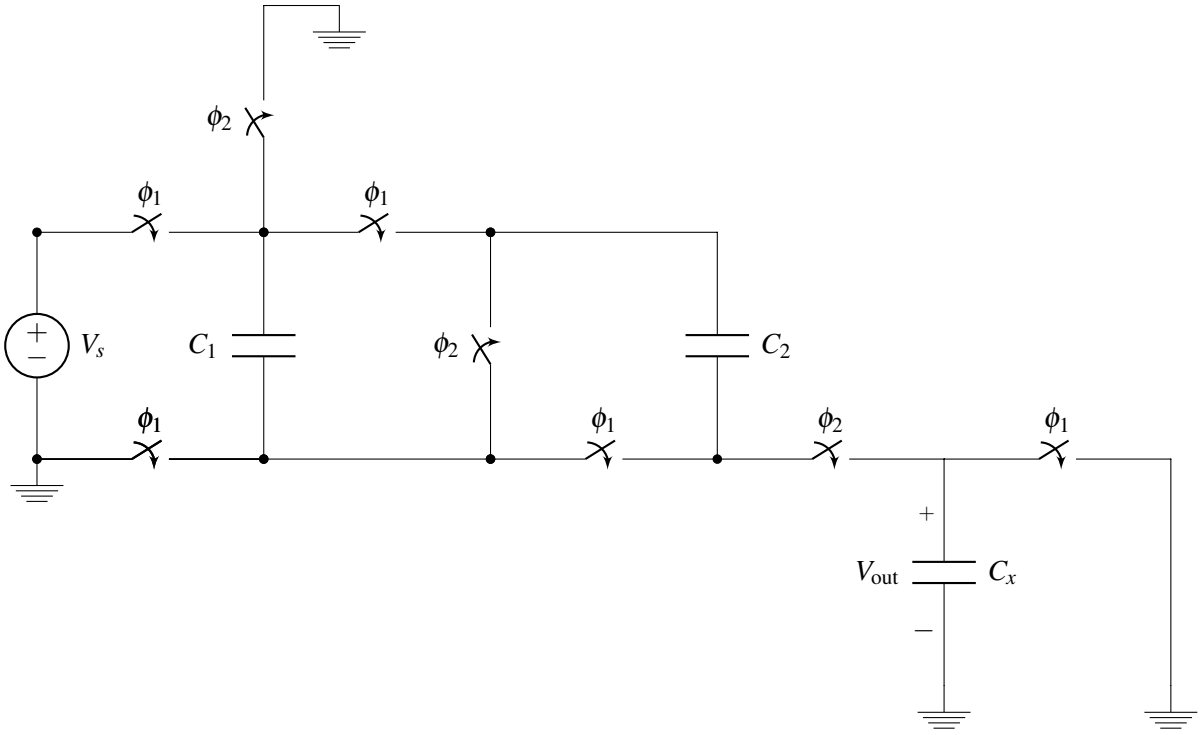
Step 6: Equate the total charge calculated in phase 1 (Step 4) to the total charge calculated in phase 2 (Step 5) (charge conservation).

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{u_3}^{\phi_2} \\ V_sC_1 &= (u_3 - V_s)C_1 + (u_3 - 0)C_2 \\ u_3 &= \frac{2C_1}{C_1 + C_2}V_s \end{aligned}$$

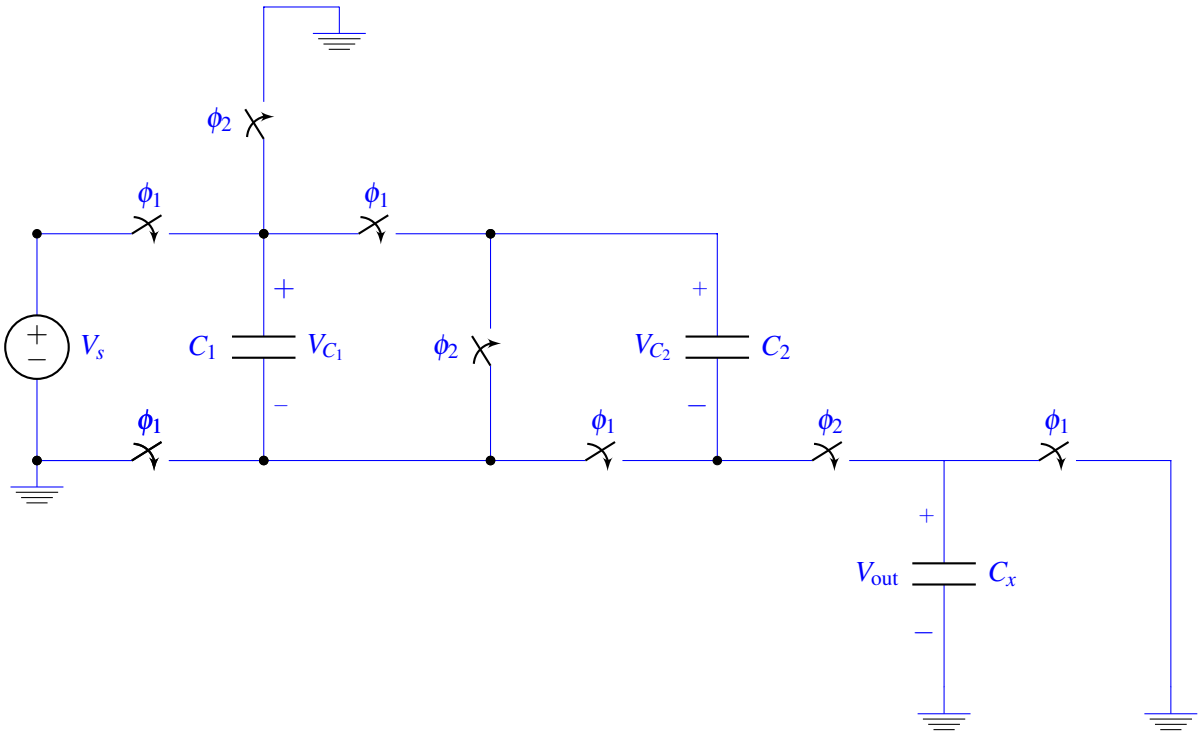
Step 7: Repeat steps 4-6 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

In this problem we did not go through step 7 since we only had one floating node during phase 2. This means we have only one unknown node voltage (u_3) for which we solved using our single equation from Step 6. We will be using step 7 in our second example!

2. Fall '19, Midterm 2: Find the voltage V_{out} across capacitor C_x at the end of phase 2, as a function of C, C_x, and V_s. Assume that $C_1 = C_2 = C$

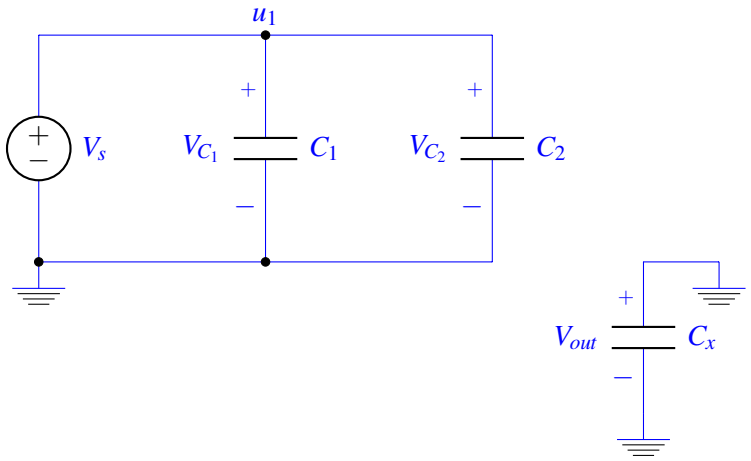


Step 1: Capacitor voltage labelling.

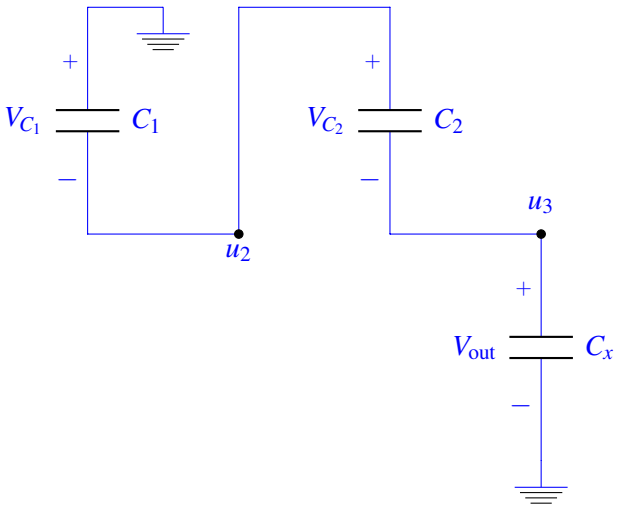


Step 2: Redrawing the circuit during both phases.

Phase 1:



Phase 2:



Step 3: Floating nodes during phase 2.

In this problem the floating nodes are u_2 and u_3 since no current is flowing into or out of them (they are only connected to capacitor plates).

Step 4: Total charge accumulated on phase 2 floating nodes during phase 1.

Let's look at u_2 first: "−" plate of C_1 and "+" plate of C_2 are connected to that node during phase 2. Calculating the charge stored in them during phase 1 we get:

$$
\begin{aligned}
Q_{u_2}^{\phi_1} &= -V_{C_1}^{\phi_1} C_1 + V_{C_2}^{\phi_1} C_2 \\
Q_{u_2}^{\phi_1} &= -(u_1 - 0)C_1 + (u_1 - 0)C_2 \\
Q_{u_2}^{\phi_1} &= -u_1 C_1 + u_1 C_2 \\
Q_{u_2}^{\phi_1} &= -V_s C_1 + V_s C_2 \\
Q_{u_2}^{\phi_1} &= 0
\end{aligned}
$$

Where in the last step we used that $C_1 = C_2 = C$ was given in the exam.

Step 5: Total charge accumulated on phase 2 floating nodes during phase 2 as a function of node voltages.

$$
\begin{aligned}
Q_{u_2}^{\phi_2} &= -V_{C_1}^{\phi_2} C_1 + V_{C_2}^{\phi_2} C_2 \\
Q_{u_2}^{\phi_2} &= -(0 - u_2)C_1 + (u_2 - u_3)C_2 \\
Q_{u_2}^{\phi_2} &= (2u_2 - u_3)C
\end{aligned}
$$

Step 6: Equate charge calculated during phases 1 and 2.

$$
\begin{aligned}
Q_{u_2}^{\phi_1} &= Q_{u_2}^{\phi_2} \\
0 &= (2u_2 - u_3)C_2
\end{aligned}
$$

$$
u_2 = \frac{u_3}{2} \tag{1}
$$

Step 7: Repeating steps 4-6 for every floating node will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

Let's repeat Steps 4-6 for node u_3:

Step 4:
u_3 is connected to the "$-$" plate of C_2 and "$+$" plate of C_x. Charge during phase 1:

$$
\begin{aligned}
Q_{u_3}^{\phi_1} &= -V_{C_2}^{\phi_1} C_2 + V_{C_x}^{\phi_1} C_x \\
&= -(u_1 - 0)C_2 + (0 - 0)C_x) \\
&= -u_1 C_2 \\
&= -V_s C
\end{aligned}
$$

Step 5: Charge during phase 2:

$$
\begin{aligned}
Q_{u_3}^{\phi_2} &= -V_{C_2}^{\phi_2} C_2 + V_{C_x}^{\phi_2} C_x \\
&= -(u_2 - u_3)C_2 + (u_3 - 0)C_x) \\
&= -u_2 C_2 + u_3 (C_x - C_2)
\end{aligned}
$$

Step 6: Equate the charge from steps 4 and 5:

$$Q_{u_3}^{\phi_1} = Q_{u_3}^{\phi_2}$$

$$-V_s C = -u_2 C + u_3 (C + C_x) \tag{2}$$

Finally, solve the system of equations (1), (2): Plugging (1) into (2) we get:

$$-V_s C = -\frac{u_3}{2} C + u_3 (C + C_x)$$
$$u_3 = -\frac{C}{\frac{C}{2} + C_x} V_s = -\frac{2V_s}{1 + \frac{2C_x}{C}}$$

And of course, $V_{out} = u_3$.

Important Notes:

(a) A node that is floating during phase 2 is not necessarily floating during phase 1. In fact, it could have been two separate nodes during phase 1 depending on how your switches are configured. We only care about the floating nodes during phase 2 since those are the nodes with unknown voltages.
What about floating nodes during phase 1? You should be able to calculate the voltage of these nodes based on the initial condition of the circuit and the circuit techniques that you have learned so far (most likely KVL).

(b) When handling charge sharing problems you should avoid using any parallel or series capacitance formulae that you have learned. Any simplification of the circuit might lead to mistakes since the circuit in different phases is configured differently and some capacitors placed in series during one phase may be in parallel or even not connected at all in another phase!