EECS 16A Designing Information Devices and Systems I
Fall 2020 Homework 9

This homework is due October 30, 2020, at 23:59.

Self-grades are due November 9, 2020, at 23:59.

Solutions for this homework will be released on Wednesday, October 28, to give you time to study for the midterm.

Submission Format

Your homework submission should consist of **one** file.

- `hw9.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).
- **We strongly recommended that you submit your self-grades PRIOR to taking Midterm 2 on Nov 2, 2020, since looking at the solutions earlier will help you to study for the midterm.**
- **Midterm 2 is on Monday, November 2nd. Please make sure you have a plan for studying for the midterm. This is the last homework in scope for the midterm. Also, please review the proctoring document to make sure you are aware of it and any changes to the policies for the exam.**

Submit the file to the appropriate assignment on Gradescope.

1. Reading Assignment

For this homework, please read Notes 16, 17 (17.1 - 17.2, specifically) and 17B. Note 16 will provide an introduction to capacitors (a circuit element which stores charge), capacitive equivalence, and the underlying physics behind them. Sections 17.1 - 17.2 in Note 17 will provide an overview of the capactive touchscreen and how to measure capacitance. Note 17B will provide a walkthrough of the charge-sharing algorithm. Section 17.3 and onwards is out of scope for the midterm

(a) Describe the key ideas behind how a capacitor works. How are capacitor equivalences calculated? Contrast this with how we calculate resistor equivalences.

(b) Consider the capacitive touchscreen. Describe how it works, and compare and contrast it to the resistive touchscreens we have seen in previous lectures and homeworks.

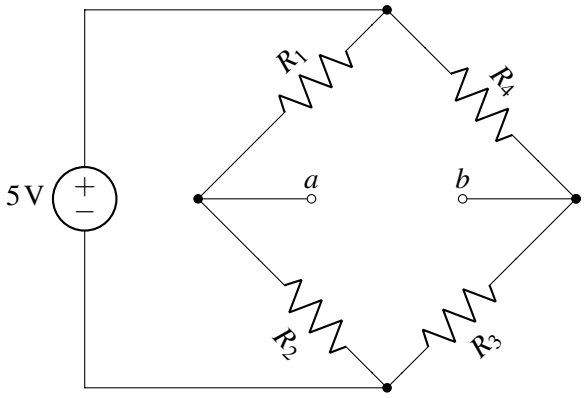
(c) What property of charge is applied in connecting phase 1 calculations to phase 2 calculations in the charge sharing algorithm?

2. Wheatstone Bridge

(Contributors: Ava Tan, Panos Zarkos)

A Wheatstone Bridge is a very useful circuit that can be used to help determine unknown resistance values with very high accuracy. This circuit is used in many sensor applications where resistors $R_1 - R_4$ are varying with respect to some external actuation. For example, it can be used to build a strain gauge (`https://en.wikipedia.org/wiki/Strain_gauge`) or a scale (remember Fruity Fred from HW 7?). In that case the resistors $R_1 - R_4$ would vary with respect to a strain caused by a force, and the Wheatstone Bridge circuit would translate that variation into a voltage difference across the "bridge" terminals a and b.

UCB EECS 16A, Fall 2020, Homework 9, All Rights Reserved. This may not be publicly shared without explicit permission.



(a) Assume that $R_1 = 2\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 1\,\text{k}\Omega$, $R_4 = 4\,\text{k}\Omega$. Calculate the voltage V_{ab} between the two terminals a and b.

Hint: You have analyzed very similar circuits in previous homeworks, in lectures, and in discussions – it may help to redraw the circuit with each branch containing resistors $R_1 - R_4$ using straight vertical wires, rather than diagonal ones.

Solution:

Notice in the above circuit that there are two voltage dividers, so we can calculate u_a and u_b quickly.

$$u_a = V_{R2} = \frac{R_2}{R_1 + R_2} \cdot 5\,\text{V} = 2.5V$$

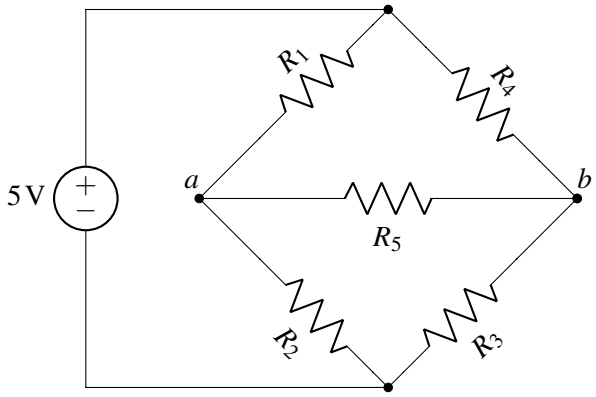
$$u_b = V_{R3} = \frac{R_3}{R_3 + R_4} \cdot 5\,\text{V} = 1V$$

Thus, the required voltage difference between the two terminals a and b is: $V_{ab} = u_a - u_b = 1.5V$.

(b) Now assume that you have added an additional resistor, R_5, between terminals a and b as shown below. Assume that $R_1 = 1\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 4\,\text{k}\Omega$, $R_4 =?\ \text{k}\Omega$, $R_5 = 4\,\text{k}\Omega$. In the process of constructing this circuit, you notice that you forgot to write down the value of R_4!

However, you notice something very curious about your Wheatstone Bridge circuit: there is no current flowing through resistor R_5.

Based on this observation, what must the value of resistor R_4 be?



Solution:

Because there is no current flowing through resistor R_5, we know that the value of V_{ab} must be zero (i.e, $u_a - u_b = 0\,\text{V}$). In other words, the nodes a and b must be at the exact same potential. We can use this fact to backtrack what the value of R_4 must be.

Since $V_{ab} = 0\,\text{V}$, we have actually two separate voltage dividers (R_1 and R_2 form one voltage divider; R_4 and R_3 form the other):

$$u_a = \frac{R_2}{R_1 + R_2} \cdot 5\,\text{V}$$
$$u_b = \frac{R_3}{R_3 + R_4} \cdot 5\,\text{V}$$
$$V_{ab} = u_a - u_b = 0 \implies \frac{R_2}{R_1 + R_2} \cdot 5\,\text{V} = \frac{R_3}{R_3 + R_4} \cdot 5\,\text{V}$$
$$\frac{R_2}{R_1 + R_2} = \frac{R_3}{R_3 + R_4}$$

Plugging in values and solving for R_4:

$$\frac{2\,\text{k}\Omega}{1\,\text{k}\Omega + 2\,\text{k}\Omega} = \frac{4\,\text{k}\Omega}{4\,\text{k}\Omega + R_4}$$
$$\implies R_4 = 2\,\text{k}\Omega$$

We note that the ratio of R_1 to R_2 turns out to be the same as the ratio of R_4 to R_3. Maintaining this ratio is what allows the voltage at node a to be equivalent to the voltage at b, and therefore for $V_{ab} = 0\,\text{V}$.

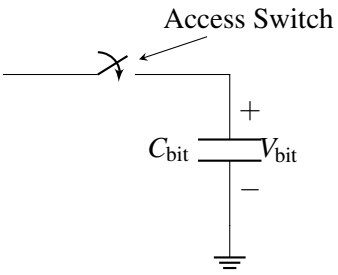
3. Dynamic Random Access Memory (DRAM)

(Contributors: Amanda Jackson, Ava Tan, Aviral Pandey, Lam Nguyen, Michael Kellman, Panos Zarkos, Titan Yuan, Vijay Govindarajan)

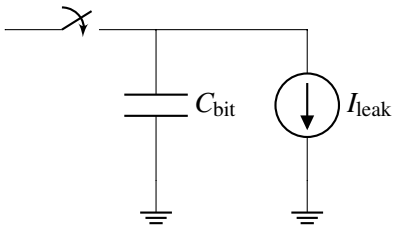
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store $>$ 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) determines whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will **model as a leakage to ground**. The figure below shows **a model of this leakage**:



Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is "written" by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

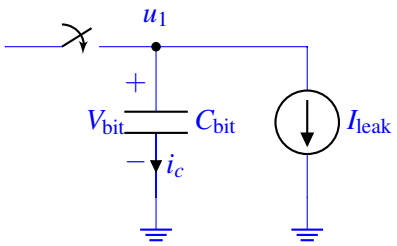
What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

Hint: Start by writing out the equations you know about charge and current related to the capacitor. Note here that the current source is discharging the capacitor.

Solution:

We want the time that a cell can read a '1' to be $t_{\text{store}} = 1\,\text{ms}$. We are given that $V_{\text{bit}}(0) = 1.2\,\text{V}$ and that $V_{\text{bit}}(1\,\text{ms}) = V_{\text{min}} = 0.9\,\text{V}$. To do this, we will first solve for the current going through the DRAM capacitor, i_c, and then solve for I_{leak}.

Labeling the voltage across the DRAM capacitor and corresponding i_c first:



We can therefore write i_c as:

$$i_c = C_{\text{bit}} \cdot \frac{dV_{\text{bit}}}{dt}$$

$$\implies \int_0^t \frac{i_c}{C_{\text{bit}}} d\tau = \int_0^t \frac{dV_{\text{bit}}}{dt} d\tau$$

$$\frac{i_c}{C_{\text{bit}}} t = V_{\text{bit}}(t) - V_{\text{bit}}(0)$$

$$\implies V_{\text{bit}}(t) = \frac{i_c}{C_{\text{bit}}} t + V_{\text{bit}}(0)$$

Substituting in $t_{\text{store}} = 1\,\text{ms}$, the initial and final voltages of V_{bit}, and $C_{\text{bit}} = 28\,\text{fF}$ and solving for i_c, we obtain:

$$\begin{aligned} V_{\text{bit}}(1\,\text{ms}) &= \frac{i_c}{C_{\text{bit}}}(1\,\text{ms}) + V_{\text{bit}}(0\,\text{ms}) \\ 0.9\,\text{V} &= \frac{i_c}{28\,\text{fF}}(1\,\text{ms}) + 1.2\,\text{V} \\ \implies i_c &= \frac{(-0.3\,\text{V})(28\,\text{fF})}{1\,\text{ms}} \\ &= -8.4\,\text{pA} \end{aligned}$$

Finally, we can solve for I_{leak} by writing a single KCL equation at node u_1.

$$\begin{aligned} i_c + I_{\text{leak}} &= 0 \\ \implies I_{\text{leak}} &= -i_c = 8.4\,\text{pA} \end{aligned}$$

4. Capacitive Touchscreen

(Contributors: Deepshika Dhanasekar, Panos Zarkos, Richard Liou, Wahid Rahman, Urmita Sikder)

The model for a capacitive touchscreen can be seen in Figure 1. See Table 1 for values of the dimensions. The green area represents the contact area of the finger with the top insulator. It has dimensions w_2 x d_1, where w_2 is the horizontal width of the finger contact area and d_1 is the depth (into the page) of the finger contact area. The top metal (red area) has dimensions $w_1 \times d_1$. The bottom metal (grey area) has dimensions $w \times d_2$, where w is larger than both w_1 and w_2.

Table 1: Touchscreen Dimension Values

d_1	10 mm
d_2	1 mm
t_1	2 mm
t_2	4 mm
w_1	1 mm
w_2	2 mm

(a) Draw the equivalent circuit of the touchscreen that contains the nodes F, E_1, and E_2 when: (i) there no finger present; and (ii) when there is a finger present. Express the capacitance values in terms of C_0, C_{F-E1}, and C_{F-E2}.

Hint: Note that node F represents the finger. When there is no touch node F would be non-existent.
Hint: Treat E_1 as the "top node", E_2 as the "bottom node", and the finger F as an intermediate node when present.

Solution:

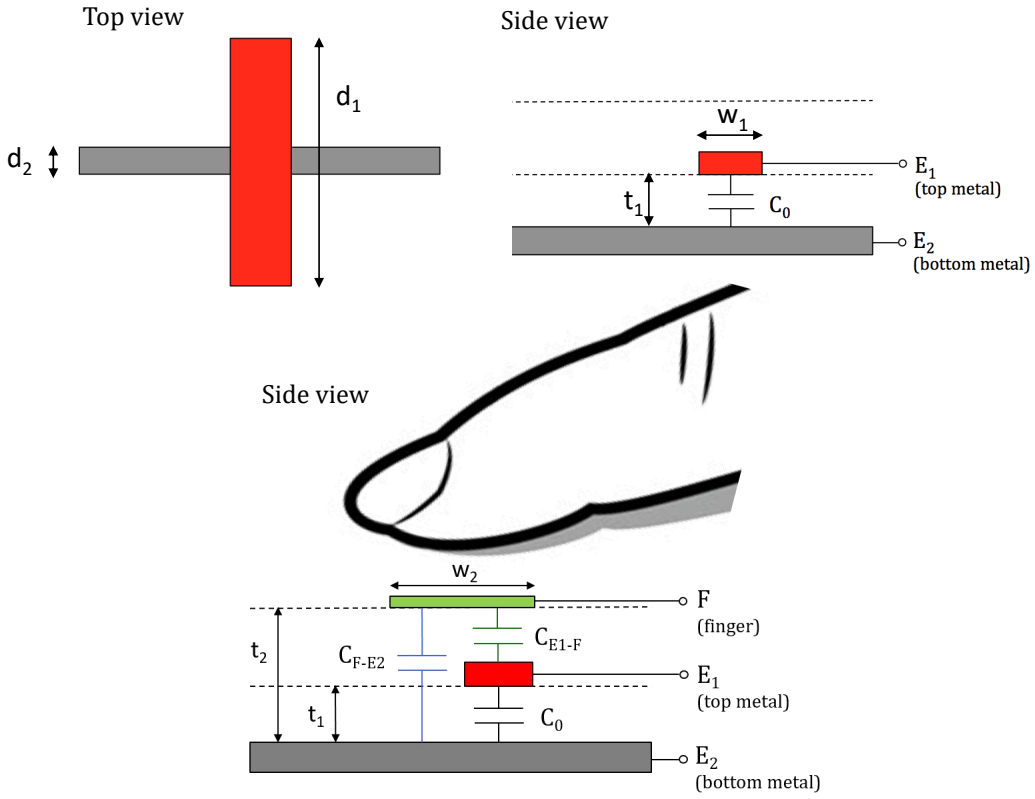


Figure 1: Model of capacitive touchscreen.

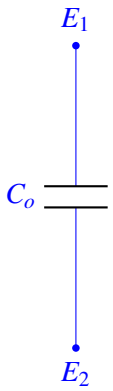


Figure 2: Touchscreen circuit with no finger present.

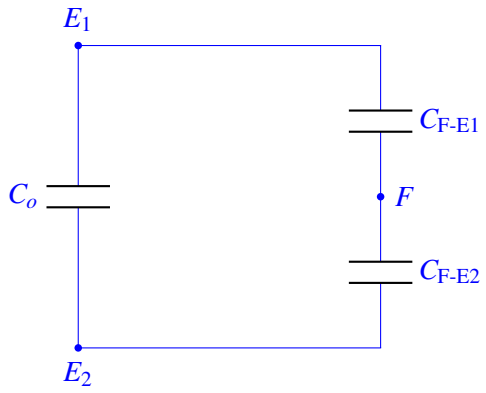


Figure 3: Touchscreen circuit with a finger present.

(b) What are the values of C_0, C_{E1-F}, and C_{F-E2}? Assume that the insulating material has a permittivity of $\varepsilon = 4.43 \times 10^{-11} F/m$ and that the thickness of the metal layers is small compared to t_1 (so you can ignore the thickness of the metal layers).

Solution:

$$C_0 = \varepsilon \frac{d_2 w_1}{t_1} = 2.215 * 10^{-14} F$$

$$C_{F-E1} = \varepsilon \frac{d_1 w_1}{t_2 - t_1} = 2.215 * 10^{-13} F$$

$$C_{F-E2} = \varepsilon \frac{d_2 (w_2 - w_1)}{t_2} = 1.108 * 10^{-14} F$$

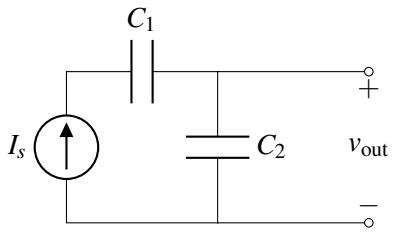
(c) What is the difference in effective capacitance between the two metal plates (nodes E_1 and E_2) when a finger is present?

Solution: The effective capacitance between the two plates is $C_0 = 2.215 * 10^{-14} F$ when there is no finger. When there is a finger, we have C_0 in parallel with a series combination of C_{F-E1} and C_{F-E2}, giving an additional capacitance $C_{F-E1} || C_{F-E2} = 1.055 * 10^{-14} F$ when a finger is present. Therefore, the total effective capacitance is: $3.270 * 10^{-14} F$.

5. More Current Sources And Capacitors

(Contributors: Ava Tan, Panos Zarkos, Wahid Rahman)

(a) For the circuit given below, give an expression for $v_{\text{out}}(t)$ in terms of I_s, C_1, C_2, and time t. Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is 0 V.



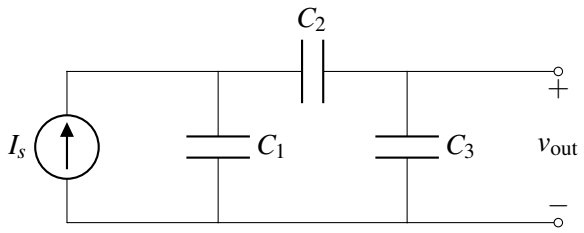
Solution:

By KCL, the current I_s flowing through C_1 must be the current flowing through C_2. $v_{\text{out}}(0) = 0$ because all capacitors are initially uncharged.

$$I_s = C_2 \frac{dv_{\text{out}}(t)}{dt}$$

$$v_{\text{out}}(t) = \int_0^t \frac{I_s}{C_2} d\tau = \frac{I_s}{C_2} t + v_{\text{out}}(0) = \frac{I_s}{C_2} t$$

(b) **(Optional, Challenge)** For the circuit given below, give an expression for $v_{\text{out}}(t)$ in terms of I_s, C_1, C_2, C_3, and t. Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is 0 V. You may choose to use either NVA or capacitor equivalences to help you solve this problem.

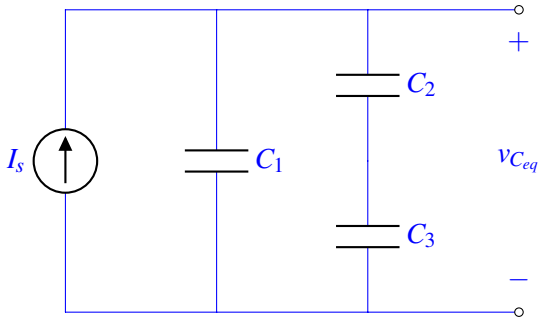


Solution:

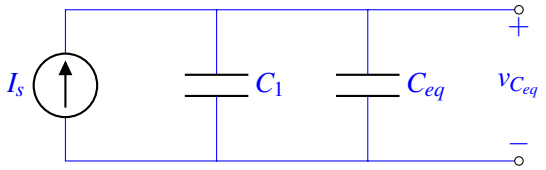
We will present two methods of calculating $v_{out}(t)$: using capacitor equivalences as well as our tried-and-true node voltage analysis technique.

1. Capacitor Equivalences

Instead of finding v_{out} directly, let's first find the voltage $v_{C_{eq}}$ across C_2 and C_3.



To do this, we recognize that C_2 and C_3 are in series. We can therefore replace them with their equivalent capacitance $C_{eq} = C_2 \parallel C_3 = \frac{C_2 C_3}{C_2 + C_3}$.



We know that to solve for $v_{C_{eq}}$, we can find the equivalent capacitance of C_1 and C_{eq} first. Since they are in parallel, we combine them as $C_1 + C_{eq}$. Since all the capacitors are initially uncharged, $v_{C_{eq}}(0) = 0$.

$$v_{C_{eq}}(t) = \int_0^t \frac{I_s}{C_1 + C_{eq}} d\tau = \frac{I_s}{C_1 + C_{eq}} t + v_{C_{eq}}(0) = \frac{I_s}{C_1 + C_{eq}} t$$

Now that we know that voltage across the equivalent capacitor C_{eq}, we can find the current flowing through the equivalent capacitor C_{eq}.

$$i_{C_{eq}}(t) = C_{eq}\frac{dv_{C_{eq}}(t)}{dt} = C_{eq}\frac{I_s}{C_1 + C_{eq}}$$

Note that the current $i_{C_{eq}}$ is equal to the current flowing through C_3 since C_2 and C_3 were originally connected in series.

$$i_{C_3}(t) = i_{C_{eq}}(t) = C_{eq}\frac{I_s}{C_1 + C_{eq}}$$

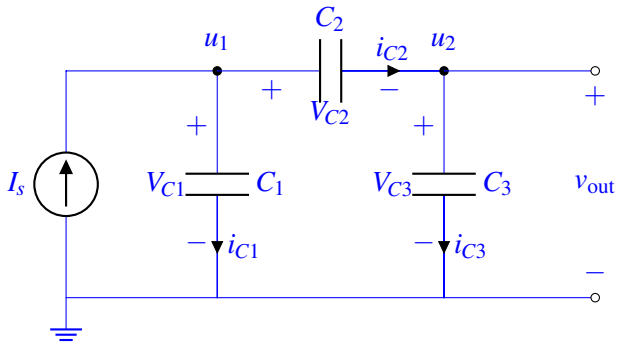
Since v_{out} is the voltage across the capacitor C_3, we integrate to find v_{out}. Again, since all capacitors are initially uncharged, $v_{\text{out}}(0) = 0$.

$$i_{C_3}(t) = C_3\frac{dv_{\text{out}}(t)}{dt}$$

$$v_{\text{out}}(t) = \int_0^t \frac{1}{C_3} C_{eq}\frac{I_s}{C_1 + C_{eq}} d\tau = \frac{C_{eq} I_s}{C_3(C_1 + C_{eq})}t + v_{\text{out}}(0) = \frac{\frac{C_2 C_3}{C_2 + C_3} I_s t}{C_3\left(C_1 + \frac{C_2 C_3}{C_2 + C_3}\right)}t = \frac{C_2 I_s}{C_1 C_2 + C_1 C_3 + C_2 C_3}t$$

2. Node Voltage Analysis

We begin by labeling our circuit in its entirety:



Writing KCL equations at u_1 and u_2 gives the following two equations:

$$u_1: \quad I_s = i_{C1} + i_{C2}$$
$$u_2: \quad i_{C2} = i_{C3}$$

Recall that differentiating the capacitor-voltage-charge relationship $Q = CV$ with respect to time gives us $\frac{dQ}{dt} = I = C \cdot \frac{dV}{dt}$. We can apply this result to our KCL equations to first solve for the *change* in v_{out}, i.e, $\frac{dV_{out}}{dt} = \frac{du_2}{dt}$, and then in the end integrate this quantity to find our final equation $v_{out}(t)$.
Rewriting our KCL equations, we obtain:

$$u_1: \quad I_s = C_1\frac{du_1}{dt} + C_2\frac{d(u_1 - u_2)}{dt}$$
$$u_2: \quad C_2\frac{d(u_1 - u_2)}{dt} = C_3\frac{du_2}{dt}$$

Let's rearrange the KCL equation for node u_2 to solve for $\frac{du_2}{dt}$.

$$C_2\frac{du_1}{dt} = (C_2+C_3)\frac{du_2}{dt}$$
$$\implies \frac{du_2}{dt} = \frac{C_2}{C_2+C_3}\frac{du_1}{dt}$$

We then plug this result into the first KCL equation written at u_1 to solve for $\frac{du_1}{dt}$:

$$\begin{aligned} I_s &= C_1\frac{du_1}{dt} + C_2\frac{du_1}{dt} - \frac{C_2^2}{C_2+C_3}\frac{du_1}{dt} \\ &= \left(C_1+C_2-\frac{C_2^2}{C_2+C_3}\right)\frac{du_1}{dt} \\ &= \left(\frac{C_1(C_2+C_3)+C_2(C_2+C_3)-C_2^2}{C_2+C_3}\right)\frac{du_1}{dt} \\ \implies \frac{du_1}{dt} &= I_s\cdot\frac{C_2+C_3}{C_1C_2+C_1C_3+C_2C_3} \end{aligned}$$

Finally, we can substitute this result back into our result for $\frac{du_2}{dt}$, which we stated earlier is equivalent to $\frac{dV_{out}}{dt}$:

$$\begin{aligned} \frac{dV_{out}}{dt} \equiv \frac{du_2}{dt} &= \frac{C_2}{C_2+C_3}\frac{du_1}{dt} \\ &= \frac{C_2}{C_2+C_3}\cdot I_s\cdot\frac{C_2+C_3}{C_1C_2+C_1C_3+C_2C_3} \\ &= I_s\cdot\frac{C_2}{C_1C_2+C_1C_3+C_2C_3} \end{aligned}$$

Lastly, we integrate $\frac{dV_{out}}{dt}$ and get our final $v_{out}(t)$ expression, which should match what was calculated using the capacitor equivalences technique.

$$\begin{aligned} v_{out}(t) &= \int_0^t \frac{dV_{out}}{dt}d\tau \\ &= \int_0^t I_s\cdot\frac{C_2}{C_1C_2+C_1C_3+C_2C_3}d\tau \\ &= \frac{I_sC_2}{C_1C_2+C_1C_3+C_2C_3}t \end{aligned}$$

6. Circuit with Capacitors

(Contributors: Ava Tan, Aviral Pandey, Lam Nguyen, Panos Zarkos, Titan Yuan)

Find the voltages at nodes A and B, and currents flowing through all of the capacitors at steady state. Assume that before the voltage source is applied, the capacitors all initially have a charge of 0 Coulombs.

In general your strategy to solve circuits with capacitors should similar to solving resistive circuits. For capacitive circuits we often care about steady state (i.e. what happens to the circuit after a long time and no more changes are happening). If we are considering a circuit with capacitors and voltage sources, we will always be thinking about steady state (or the steady state for a phase if are are doing a charge sharing

problem with switches). When thinking about steady state you always want to write out the equations for charge that you know, as well as all the KVL type relationships around voltages you know. Then use the key idea that charge is conserved to build out your system of equations. Don't be daunted by the variable names and know that everything just boils down to a system of linear equations.

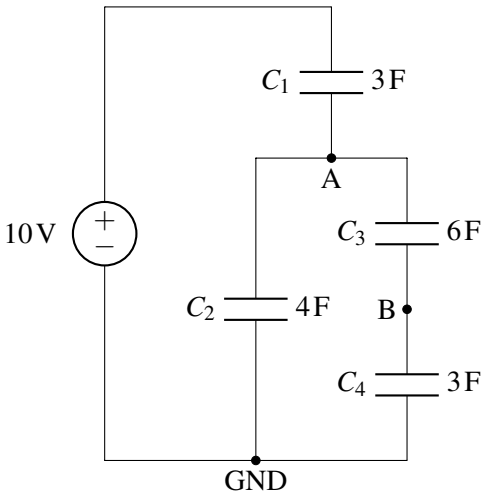
Here are some principles that are also helpful:

(a) Charge at a node from which charge cannot escape or enter is always conserved. — if the sum of charges is 0 on a node, the sum of charges on that node at steady state will be zero.

(b) The charge Q stored in a capacitor is given by the equation $Q = CV$.That is, the plate that corresponds to the "+" terminal, stores $+Q = +CV$, and the plate that corresponds to the "-" terminal, stores $-Q = -CV$.

(c) If two capacitors are initially uncharged, and then are connected in series, the charges on both capacitors are equal to each other at steady state.

(d) The voltage across capacitors in parallel is equal at steady state.



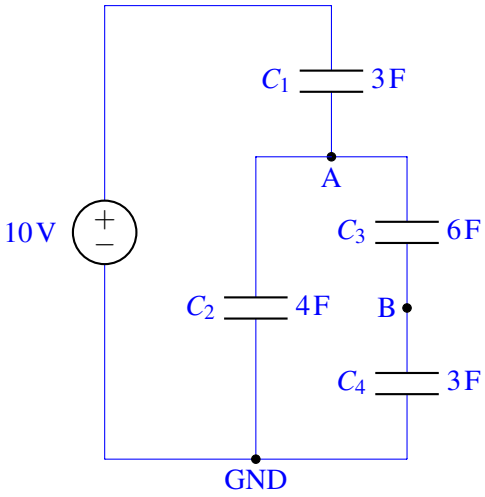
Solution:

Method 1: Charge conservation

For a capacitor C_k, let us denote the voltage across it by v_{C_k}, the current flowing through it by i_{C_k}, and its charge by Q_{C_k}. In steady state (that is, after the current has been running for a very long time), direct current (DC) capacitors act as open circuits. Hence, we see that there is no current flowing through the capacitors, that is,

$$i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0\,\text{A}.$$

For finding the voltages across the capacitors, let us label nodes on the circuit as shown in the following figure.



We are going to use the following four properties to find the voltages across the capacitors:

(a) Charge is always conserved.
(b) The charge Q stored in a capacitor is given by the equation $Q = CV$.
(c) The charges across series capacitors are equal to each other.
(d) The voltage across parallel capacitors is equal.

As an example use of property (c), we have the charge on the capacitor C_3 equal to the charge on the capacitor C_4.

Let us start by writing the equation for conservation of charge at node A:

$$Q_{C_1} = Q_{C_2} + Q_{C_3}$$

By property (b), that is, $Q = CV$, we can equivalently write this equation for charge conservation in terms of node voltages as

$$(10\,\text{V} - v_A)3\,\text{F} = v_A 4\,\text{F} + (v_A - v_B)6\,\text{F},$$

which, after simplifying the equation, gives

$$30\,\text{V} = 13v_A - 6v_B. \tag{1}$$

Let us then write the charge conservation equation at node B; we have

$$Q_{C_3} = Q_{C_4}.$$

As before, we can write this charge conservation equation in terms of the node voltages as

$$(v_A - v_B)6\,\text{F} = v_B 3\,\text{F},$$

which, after simplification, gives

$$2v_A = 3v_B. \tag{2}$$

Equations 1 and 2 give us two linearly independent equations in two unknowns. Solving the system, we get

$$v_A = \frac{10}{3}\,\text{V},$$
$$v_B = \frac{20}{9}\,\text{V}.$$

Using the node voltages, we can calculate the voltages across the capacitors as

$$v_{C_1} = 10\,\text{V} - v_A = \frac{20}{3}\,\text{V},$$
$$v_{C_2} = v_A = \frac{10}{3}\,\text{V},$$
$$v_{C_3} = v_A - v_B = \frac{10}{9}\,\text{V},$$
$$v_{C_4} = v_B = \frac{20}{9}\,\text{V}.$$

We write the currents across the capacitors again here for reader's convenience:

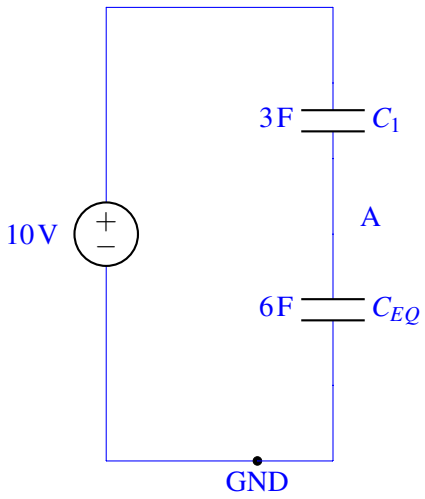
$$i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0\,\text{A}$$

Method 2: Capacitor equivalence

Let's try to consider another method of solving this. We know that, initially, all the capacitors have charges of 0 C. After a 10 V voltage source is applied, the intermediate node voltages v_A and v_B will settle to some steady-state value.

Note that capacitor voltage division only works here because we know the initial conditions of the capacitors before and after the 10 V voltage source is applied. Capacitor voltage division is really just another way of solving for charge redistribution.

Let's try to find the voltage v_A.



Note that we replaced the capacitors below node A with an equivalent capacitance $C_{EQ} = (6\,\text{F} \parallel 3\,\text{F}) + 4\,\text{F} = 6\,\text{F}$ (can you prove to yourself why?). The equation for v_A uses the *capacitor* voltage division formula:

$$v_A = 10\,\text{V}\frac{3\,\text{F}}{3\,\text{F}+6\,\text{F}} = \frac{10}{3}\,\text{V}$$

We can then recognize that the voltage v_B is the capacitor voltage division of v_A, namely:

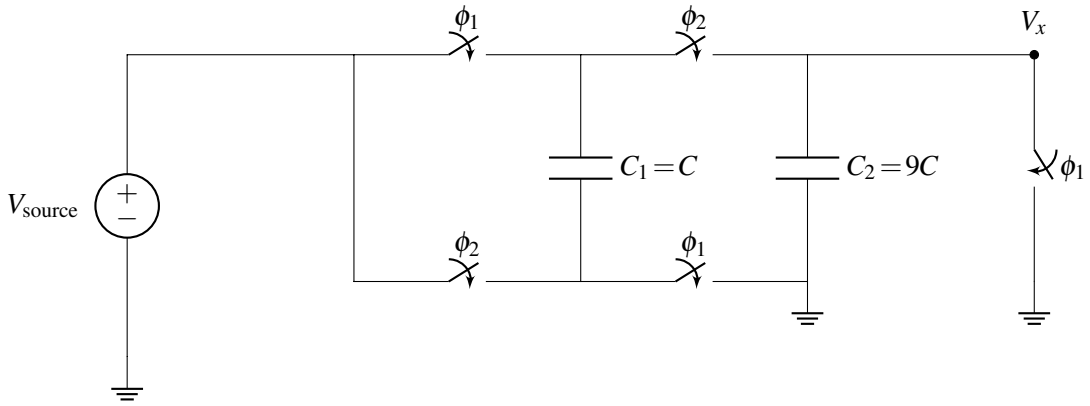
$$v_B = \frac{6\text{F}}{6\text{F}+3\text{F}} v_A$$
$$= (\frac{2}{3})\frac{10}{3}\text{V}$$
$$= \frac{20}{9}\text{V}$$

Note that these are the same values we found using Method 1.

7. Charge Sharing

(Contributors: Amanda Jackson, Ava Tan, Deepshika Dhanasekar, Moses Won, Panos Zarkos, Wahid Rahman)

Consider the following circuit:



In the first phase, all of the switches labeled ϕ_1 will be closed and all switches labeled ϕ_2 will be open. In the second phase, all switches labeled ϕ_1 are opened and all switches labeled ϕ_2 are closed.

(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

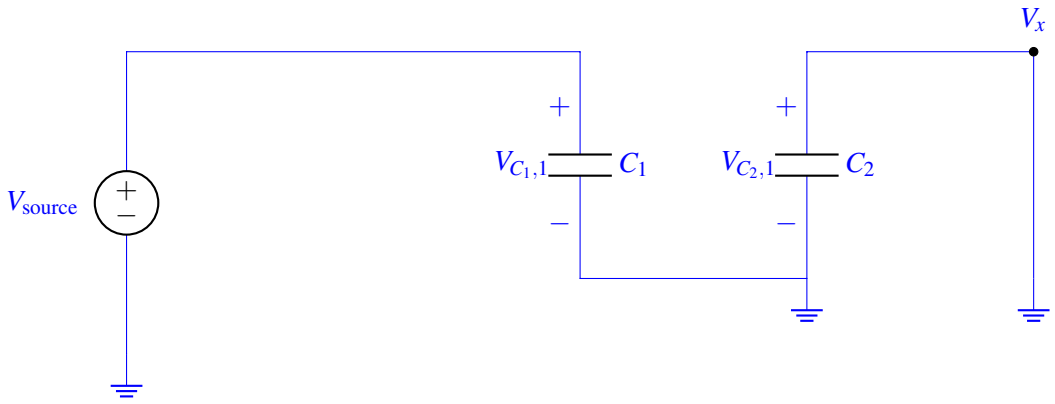
Solution:

One way of marking the polarities is + on the top plate and − on the bottom plate of both C_1 and C_2. Let's call the voltage drop across C_1 V_{C_1} and across C_2 V_{C_2}.

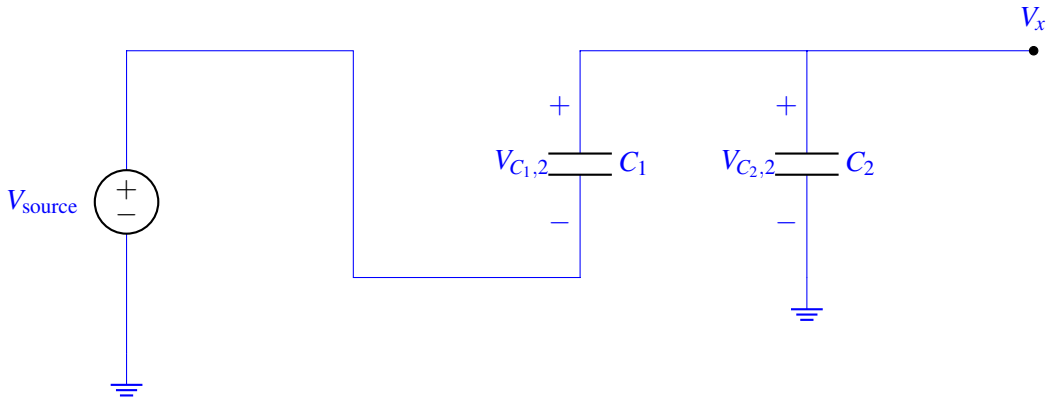
(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

Solution:

Phase 1



Phase 2



In phase 1, all the switches marked as ϕ_1 are closed and switches marked as ϕ_2 are open. In phase 2, all the switches marked as ϕ_2 are closed and switches marked as ϕ_1 are open. Draw both the circuits separately, side by side, with the switches in their respective positions.

(c) Find the voltage across and the charge on C_1 and C_2 in phase 1. Be sure to keep the polarities of the voltages the same!

Solution:

In phase 1,

$$V_{C_1,1} = V_{\text{source}} - 0 = V_{\text{source}}$$

and

$$V_{C_2,1} = 0 - 0 = 0$$

Next, we find the charge on each capacitor in phase 1:

$$Q_{C_1,1} = V_{C_1,1} C_1 = C V_{\text{source}}$$

Note that the positive plate has a charge of $+CV_{\text{source}}$, while the negative plate has a charge of $-CV_{\text{source}}$.

$$Q_{C_2,1} = V_{C_2,1} C_2 = 0$$

(d) Now, in the second phase, find the voltage V_x.

Solution:

Where is charge conserved? To answer this, look at the top plates of C_1 and C_2. In phase 2, they are both "floating" because they are not connected to V_{source} or ground. And in phase 1, they are not

connected to each other, but in phase 2, they are connected by the switch. Therefore, in phase 2, the charges on the top plates of C_1 and C_2 will be *shared*, or distributed, because they simply cannot go anywhere else. The total charge will remain the same as in phase 1. Let's find the voltages across C_1 and C_2 in phase 2 (same polarities as in phase 1!):

$$V_{C_1,2} = V_x - V_{\text{source}}$$

and

$$V_{C_2,2} = V_x$$

Now, let's find the charge stored in top plates of C_1 and C_2:

$$Q_{C_1,2} = C(V_x - V_{\text{source}})$$

and

$$Q_{C_2,2} = 9CV_x$$

Next, let's write the equation for charge conservation:

$$Q_{C_1,1} + Q_{C_2,1} = Q_{C_1,2} + Q_{C_2,2},$$

giving

$$CV_{\text{source}} + 0 = C(V_x - V_{\text{source}}) + 9CV_x,$$

which results in

$$V_x = \frac{V_{\text{source}}}{5}.$$

(e) If the capacitor C_2 did not exist (i.e. had a capacitance of 0F), what would the voltage V_x be?

Solution:

We could always go back to the equations above, plug in $C_2 = 0$, and derive $V_x = 2V_{\text{source}}$. It might be worthwhile to go over what this means for the circuit, though. If $C_2 = 0$F, the capacitor is actually an open circuit. (*Why?*) So we can pretend, as the question says, that C_2 does not exist. In phase 1, as before, C_1 has a voltage drop of V_{source} across it (from top to bottom) and is charged up to CV_{source}. Now, in phase 2, the top plate of C_1 is left dangling (floating). This means that the charge on the top plate of C_1 is going to be the same just like the charge on the bottom plate. We will therefore get

$$V_x = V_{\text{source}} - (-V_{\text{source}}) = 2V_{\text{source}}$$

Intuitively, we can think of the capacitor C_1 as a "temporary battery". In phase 1, C_1 is charged with a certain $Q = C_1V_{\text{source}}$. In phase 2, when $C_2 = 0$ (i.e. doesn't exist), the node V_x is floating and so the charge on C_1 has nowhere to go. In other words, the charge on C_1 does not change, so the voltage across C_1 does not change. This means that there is a voltage increase of V_{source} from its bottom plate to top plate. Now that the bottom plate is connected to V_{source}, that means its top plate must have a value of $2V_{\text{source}}$.

If there were no resistive losses in the circuit, this "temporary battery" would set $V_x = 2V_{\text{source}}$ forever. However, any real circuit has some resistances (either by design or due to unintended switch resistances), and these resistances will "drain" the battery and decay the voltage V_x over time. You will learn more about this transient decay (time constants) in EECS16B.

Recipe for charge sharing:

i. Label the voltages across all the capacitors. Choose whichever direction (polarity) you want foreach capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "-" sign. Just make sure you stay consistent with this polarity across phases.

ii. Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the Phase 1 circuit might be merged or split in Phase 2.

iii. Identify all "floating" nodes in your circuit during Phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op-amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.

iv. Pick a floating node from the ones you found in Step 3 and identify all capacitor plates connected to that node during Phase 2. Then, calculate the charge on each of these plates during Phase 1. To do so, identify all nodes in your circuit during Phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (Step 2 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage across a capacitor).

v. Find the total charge on each of the floating nodes during Phase 2 as a function of node voltages. Use the same process as in Step 4, but this time using the node voltages during Phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

vi. Equate the total charge calculated in Phase 1 (Step 4) to the total charge calculated in Phase 2 (Step 5) (charge conservation).

vii. Repeat Steps 4-6 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during Phase 2 (unknowns). It should have a unique solution!

As you probably noticed this exercise was architected in a way that basically walked you through this recipe used to approach charge sharing problems.

8. Preparing for Midterm 2. (No submission required.)

Please be sure to again review and be familiar with the entirety of the EECS16A exam proctoring policy (click here) before the second midterm on **November 2, 2020**. We recommend doing this well in advance of the midterm. No submission is required for this question. Given our limited TA hours, we may not be able to answer logistical and other questions over the weekend/right before the midterm. Please do ask your questions in advance to make sure we are able to answer them — thanks for understanding!

9. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

Solution:

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.