EECS 16A Designing Information Devices and Systems I
Fall 2020 Homework 9

This homework is due October 30, 2020, at 23:59.

Self-grades are due November 9, 2020, at 23:59.

Solutions for this homework will be released on Wednesday, October 28, to give you time to study for the midterm.

Submission Format

Your homework submission should consist of **one** file.

- `hw9.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).
- **We strongly recommended that you submit your self-grades PRIOR to taking Midterm 2 on Nov 2, 2020, since looking at the solutions earlier will help you to study for the midterm.**
- **Midterm 2 is on Monday, November 2nd. Please make sure you have a plan for studying for the midterm. This is the last homework in scope for the midterm. Also, please review the proctoring document to make sure you are aware of it and any changes to the policies for the exam.**

Submit the file to the appropriate assignment on Gradescope.

1. Reading Assignment

For this homework, please read Notes 16, 17 (17.1 - 17.2, specifically) and 17B. Note 16 will provide an introduction to capacitors (a circuit element which stores charge), capacitive equivalence, and the underlying physics behind them. Sections 17.1 - 17.2 in Note 17 will provide an overview of the capactive touchscreen and how to measure capacitance. Note 17B will provide a walkthrough of the charge-sharing algorithm. Section 17.3 and onwards is out of scope for the midterm

(a) Describe the key ideas behind how a capacitor works. How are capacitor equivalences calculated? Contrast this with how we calculate resistor equivalences.

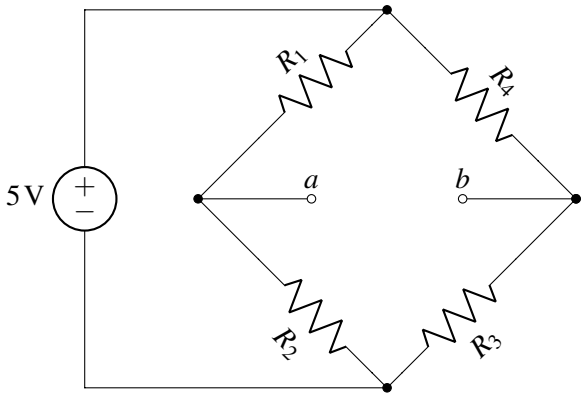
(b) Consider the capacitive touchscreen. Describe how it works, and compare and contrast it to the resistive touchscreens we have seen in previous lectures and homeworks.

(c) What property of charge is applied in connecting phase 1 calculations to phase 2 calculations in the charge sharing algorithm?

2. Wheatstone Bridge

(Contributors: Ava Tan, Panos Zarkos)

A Wheatstone Bridge is a very useful circuit that can be used to help determine unknown resistance values with very high accuracy. This circuit is used in many sensor applications where resistors $R_1 - R_4$ are varying with respect to some external actuation. For example, it can be used to build a strain gauge (`https://en.wikipedia.org/wiki/Strain_gauge`) or a scale (remember Fruity Fred from HW 7?). In that case the resistors $R_1 - R_4$ would vary with respect to a strain caused by a force, and the Wheatstone Bridge circuit would translate that variation into a voltage difference across the "bridge" terminals a and b.



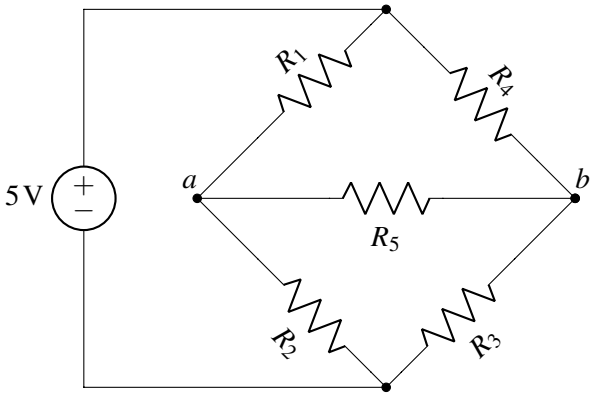
(a) Assume that $R_1 = 2\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 1\,\text{k}\Omega$, $R_4 = 4\,\text{k}\Omega$. Calculate the voltage V_{ab} between the two terminals a and b.

Hint: You have analyzed very similar circuits in previous homeworks, in lectures, and in discussions – it may help to redraw the circuit with each branch containing resistors $R_1 - R_4$ using straight vertical wires, rather than diagonal ones.

(b) Now assume that you have added an additional resistor, R_5, between terminals a and b as shown below. Assume that $R_1 = 1\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 4\,\text{k}\Omega$, $R_4 =?$ kΩ, $R_5 = 4\,\text{k}\Omega$. In the process of constructing this circuit, you notice that you forgot to write down the value of R_4!

However, you notice something very curious about your Wheatstone Bridge circuit: there is no current flowing through resistor R_5.

Based on this observation, what must the value of resistor R_4 be?



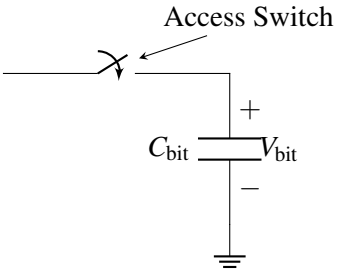
3. Dynamic Random Access Memory (DRAM)

(Contributors: Amanda Jackson, Ava Tan, Aviral Pandey, Lam Nguyen, Michael Kellman, Panos Zarkos, Titan Yuan, Vijay Govindarajan)

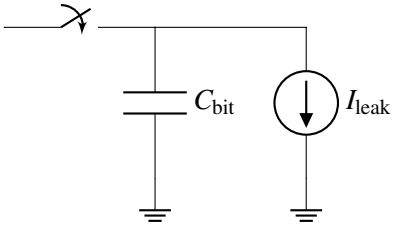
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) determines whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will **model as a leakage to ground**. The figure below shows **a model of this leakage**:



Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is "written" by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

Hint: Start by writing out the equations you know about charge and current related to the capacitor. Note here that the current source is discharging the capacitor.

4. Capacitive Touchscreen

(Contributors: Deepshika Dhanasekar, Panos Zarkos, Richard Liou, Wahid Rahman, Urmita Sikder)

The model for a capacitive touchscreen can be seen in Figure 1. See Table 1 for values of the dimensions. The green area represents the contact area of the finger with the top insulator. It has dimensions w_2 x d_1, where w_2 is the horizontal width of the finger contact area and d_1 is the depth (into the page) of the finger contact area. The top metal (red area) has dimensions $w_1 \times d_1$. The bottom metal (grey area) has dimensions $w \times d_2$, where w is larger than both w_1 and w_2.

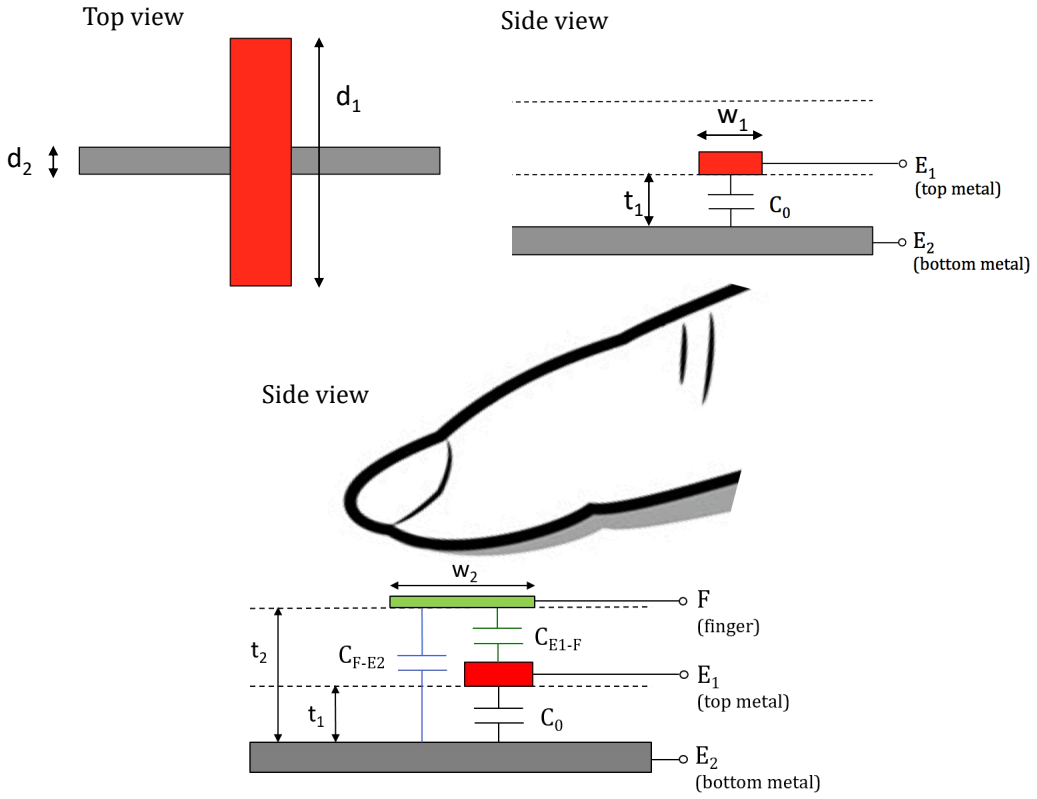


Figure 1: Model of capacitive touchscreen.

(a) Draw the equivalent circuit of the touchscreen that contains the nodes F, E_1, and E_2 when: (i) there no finger present; and (ii) when there is a finger present. Express the capacitance values in terms of C_0, C_{F-E1}, and C_{F-E2}.
Hint: Note that node F represents the finger. When there is no touch node F would be non-existent.
Hint: Treat E_1 as the "top node", E_2 as the "bottom node", and the finger F as an intermediate node when present.

(b) What are the values of C_0, C_{E1-F}, and C_{F-E2}? Assume that the insulating material has a permittivity of $\varepsilon = 4.43 \times 10^{-11} F/m$ and that the thickness of the metal layers is small compared to t_1 (so you can ignore the thickness of the metal layers).

(c) What is the difference in effective capacitance between the two metal plates (nodes E_1 and E_2) when a finger is present?

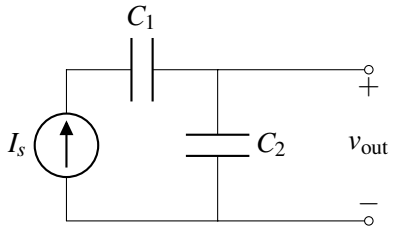
5. More Current Sources And Capacitors

(Contributors: Ava Tan, Panos Zarkos, Wahid Rahman)

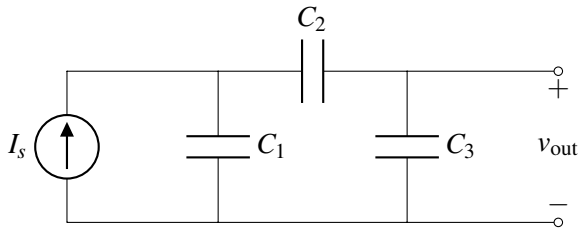
(a) For the circuit given below, give an expression for $v_{\text{out}}(t)$ in terms of I_s, C_1, C_2, and time t. Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is 0 V.

Table 1: Touchscreen Dimension Values

d_1	10 mm
d_2	1 mm
t_1	2 mm
t_2	4 mm
w_1	1 mm
w_2	2 mm



(b) **(Optional, Challenge)** For the circuit given below, give an expression for $v_{\text{out}}(t)$ in terms of I_s, C_1, C_2, C_3, and t. Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is 0 V. You may choose to use either NVA or capacitor equivalences to help you solve this problem.



6. Circuit with Capacitors

(Contributors: Ava Tan, Aviral Pandey, Lam Nguyen, Panos Zarkos, Titan Yuan)

Find the voltages at nodes A and B, and currents flowing through all of the capacitors at steady state. Assume that before the voltage source is applied, the capacitors all initially have a charge of 0 Coulombs.

In general your strategy to solve circuits with capacitors should similar to solving resistive circuits. For capacitive circuits we often care about steady state (i.e. what happens to the circuit after a long time and no more changes are happening). If we are considering a circuit with capacitors and voltage sources, we will always be thinking about steady state (or the steady state for a phase if are are doing a charge sharing problem with switches). When thinking about steady state you always want to write out the equations for charge that you know, as well as all the KVL type relationships around voltages you know. Then use the key idea that charge is conserved to build out your system of equations. Don't be daunted by the variable names and know that everything just boils down to a system of linear equations.

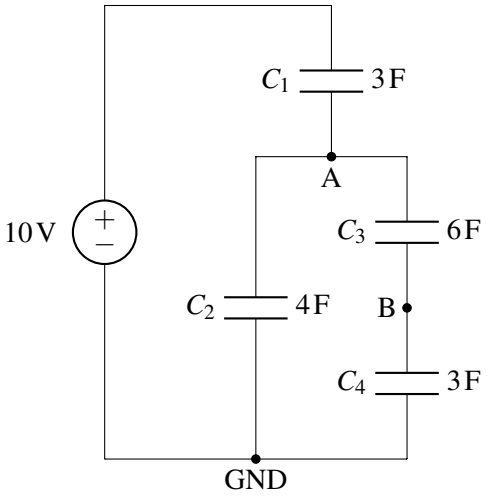
Here are some principles that are also helpful:

(a) Charge at a node from which charge cannot escape or enter is always conserved. — if the sum of charges is 0 on a node, the sum of charges on that node at steady state will be zero.

(b) The charge Q stored in a capacitor is given by the equation $Q = CV$.That is, the plate that corresponds to the "+" terminal, stores $+Q = +CV$, and the plate that corresponds to the "-" terminal, stores $-Q = -CV$.

(c) If two capacitors are initially uncharged, and then are connected in series, the charges on both capacitors are equal to each other at steady state.

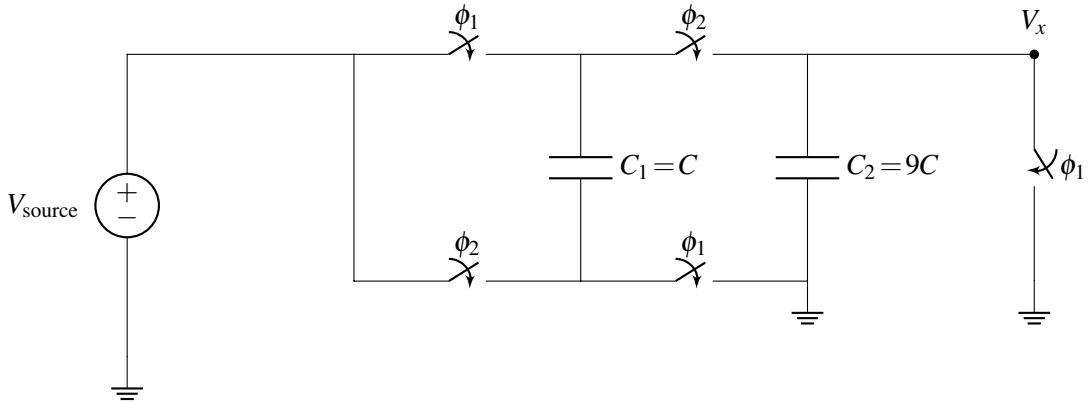
(d) The voltage across capacitors in parallel is equal at steady state.



7. Charge Sharing

(Contributors: Amanda Jackson, Ava Tan, Deepshika Dhanasekar, Moses Won, Panos Zarkos, Wahid Rahman)

Consider the following circuit:



In the first phase, all of the switches labeled ϕ_1 will be closed and all switches labeled ϕ_2 will be open. In the second phase, all switches labeled ϕ_1 are opened and all switches labeled ϕ_2 are closed.

(a) Draw the polarity of the voltage (using $+$ and $-$ signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label $+$ or $-$; just remember to keep these consistent through phase 1 and 2!)

(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

(c) Find the voltage across and the charge on C_1 and C_2 in phase 1. Be sure to keep the polarities of the voltages the same!

(d) Now, in the second phase, find the voltage V_x.

(e) If the capacitor C_2 did not exist (i.e. had a capacitance of 0 F), what would the voltage V_x be?

8. Preparing for Midterm 2. (No submission required.)

Please be sure to again review and be familiar with the entirety of the EECS16A exam proctoring policy (click here) before the second midterm on **November 2, 2020**. We recommend doing this well in advance of the midterm. No submission is required for this question. Given our limited TA hours, we may not be able to answer logistical and other questions over the weekend/right before the midterm. Please do ask your questions in advance to make sure we are able to answer them — thanks for understanding!

9. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

