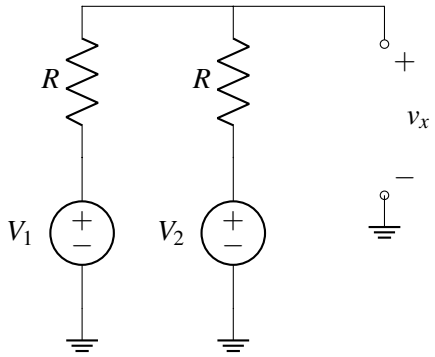
EECS 16A Designing Information Devices and Systems I
Spring 2019 Discussion 10A

1. Practice: Dividers for Days

(a) Solve the following circuit for v_x.



Answer: Using superposition and employing the voltage divider equation twice, we get:

$$v_x = \frac{1}{2}V_1 + \frac{1}{2}V_2$$

(b) You have access to two voltage sources, V_1 and V_2. You can use two resistors (as long as $0 \leq R < \infty$). How would you design a circuit that produces a voltage $v_x = \frac{1}{3}V_1 + \frac{2}{3}V_2$?

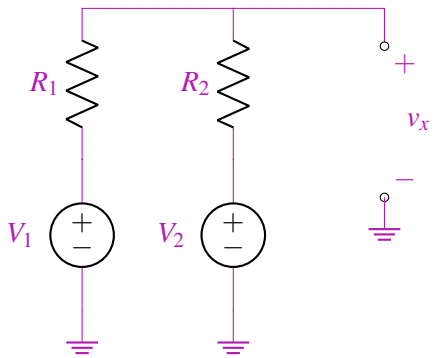
Answer:

Using superposition, we can find the output voltage for any two resistors R_1 and R_2 as:

$$v_x = \frac{R_2}{R_1 + R_2}V_1 + \frac{R_1}{R_1 + R_2}V_2$$

Thus, to create the $\frac{1}{3}$ - $\frac{2}{3}$ ratio, we can use any nonzero resistances with value R such that:

$$R_1 = 2R \qquad R_2 = R$$

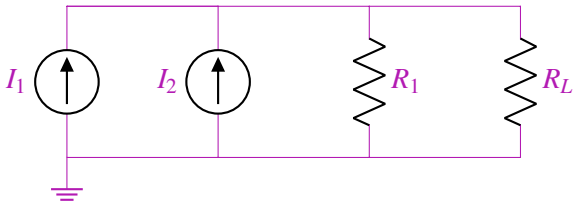


(c) You have two current sources I_1 and I_2. You also have a load resistor $R_L = 6\,\text{k}\Omega$. Similar to the first part, you can use whatever resistors you want (as long as they are finite integer multiples of $1\,\text{k}\Omega$). How would you design a circuit such that the current running through R_L is $I_L = \frac{2}{5}(I_1 + I_2)$?

Answer:

Use superposition, so think of the two currents as one summed current. Then, use KCL to determine how to divide the currents. Remember, the current divider formula is similar to that of the voltage divider, with the numerators flipped. This means that in the current divider, when calculating the current through one resistor we place the other resistor in the numerator, i.e.:

$$I_{R1} = \frac{R_L}{R_1 + R_L}(I_1 + I_2), \quad I_{R_L} = \frac{R_1}{R_1 + R_L}(I_1 + I_2)$$

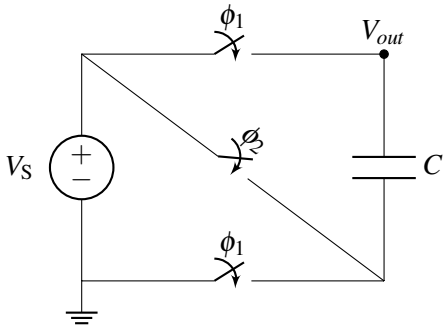


Using the above equations, we get that one possible resistor combination that creates $I_L = \frac{2}{5}(I_1 + I_2)$ is:

$$R_L = 6\,\text{k}\Omega, R_1 = 4\,\text{k}\Omega$$

2. Voltage Booster

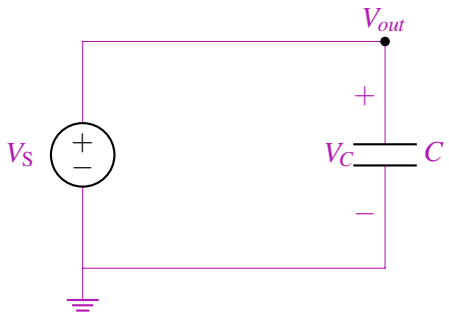
We have made extensive use of resistive voltage dividers to reduce voltage. What about a circuit that boosts voltage to a value greater than the supply $V_S = 5V$? We can do this with capacitors!



(a) In the circuit above switches ϕ_1 are initially closed and switch ϕ_2 is initially open. Calculate the value of the output voltage, V_{out} with respect to ground, and the amount of charge stored on capacitor, C, at that state (phase 1).

Answer:

In this setting we have the following equivalent circuit:



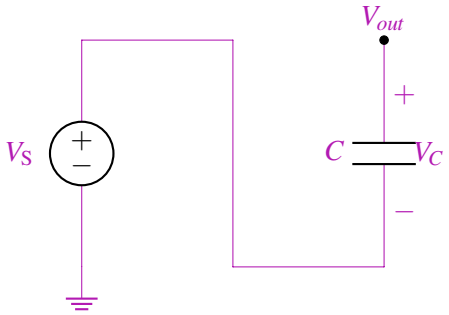
Hence,

$$V_{out} = V_S, \quad Q = CV_S.$$

(b) Now, after the capacitors are charged, switches ϕ_1 are opened and switch ϕ_2 is closed. Calculate the new voltage output voltage, V_{out}, at steady state.

Answer:

Phase 2 equivalent ckt:



In phase 2 notice that the voltage source is connected to the *negative* plate of capacitor C, while the positive plate is left floating (since it is open). Hence, charge is going to be conserved on the top plate of C. However, in phase 2: $V_C^{\phi_2} = V_{out} - V_S$:

$$Q_C^{\phi_1} = Q_C^{\phi_2} \Rightarrow CV_S = C(V_{out} - V_S) \Rightarrow V_out = 2V_S = 10V!$$

We have created a voltage doubler!